SYMBOL SYNCHRONIZATION FOR DATA COMMUNICATIONS

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By
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CERTIFICATE

Certified that this work on "SYMBOL SYNCHRONIZATION FOR DATA COMMUNICATIONS" by Mr. A. Rama Rao has been carried out under my supervision and that this has not been submitted elsewhere for a degree.

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A. RAMA RAO

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABSTRACT

For an accurate and efficient transmission of data signals we have to resort to synchronous communications. Symbol synchronization is the first level of synchronization which pertains to the base band data signals.

After studying different methods of synchronization and variations of error probability with timing deviations a symbol synchronizer has been constructed. The technique is based on phase locked loop. The comparator used is a sawtooth comparator, because of its inherently large linear range and the assosiated advantages.

The symbol synchronizer constructed was tested with data signals, generated using a 1 MHz clock eventhough it can be used safely upto 10 MHz. The synchronizer can be made to lock to the desired data frequency by varying the frequency of the voltage controlled oscillator.

CHAPTER 1

INTRODUCTION

With the increasing demand for Digital Communication world over, synchronization problems - analysis and their hardware solutions - are getting considerable attention. The present thesis reviews various synchronization techniques and describes a particular method for symbol synchronization. This has also been realized with the use of IC chips. Synchronization problem becomes important in digital communication because of the obvious reasons that the receiver must be able to decode the message properly. Various levels of synchronization are to be satisfied for proper recovery of the message; for example, while demodulating a received signal in a band pass system, an exact knowledge of the local oscillator frequency and phase is essential for optimum quality of reception. This is achieved if one maintains carrier synchronization. We are interested in synchronous communication systems only.

The first level of synchronization that appears in the synchronous communications is that of carrier synchronization. If the transmitter and the receiver clocks are highly stable, this level of synchronization can be eliminated

However, owing to the difficulty in acheiving high stability in clocks as well as the high cost of these clocks, it is required to transmit the clock signal for accurate synchronizatio After the carrier synchronization come the other levels of synchronization such as symbol, word and frame synchronization. These synchronizations pertain to the base band data signals.

In practice the messages are transmitted as code words of suitable block codes. These code words consists of a fixed number of elamentary symbols. The decoder takes a decision for each symbol and then another decision for the code word. This process requires two levels of synchronization, the symbol and word synchronizations. A number of successive code words form a frame. Another decision has to be taken by the decoder for the frame. This requires frame synchronization.

A message structure is said to symbol synchronous if the symbols of the code word are having equal duration.

A message structure is said to be Word Synchronous if the duration of the code words in the message frame is of equal duration, if not multiples of at least the maximum duration of the code word.

A message structure is said to be Frame Synchronous if the duration of the message is at least the multiple of the maximum duration of the message frame i.e. the duration

of each frame in the message is equal to at least the multiple of a frame.

A message structure is simply called synchronous if it is symbol, word and frame synchronous.

A typical counter example of message structure which is word asynchronous but symbol synchronous is the conventional telex system. Whereas synchronous message structures are found in PCM systems, telemetry and data transmission systems. In the above systems some relationship exists between symbol, word and frame synchronization. Let us study these synchronizations in block code decoders as the messages are usually transmitted as block codes.

Synchronization in Block Code Decoders:

A conventional block code decoder is shown in Fig. 1.1. The symbols are of equal duration and the word duration is a multiple of symbol duration and frame duration is a multiple of that of words. The above property can readily be used for the implementation of synchronization in block code decoders at all levels.

The setup in Fig. 1.1 can be considered as the extension of a linear receiver. The linear part of the receiver is connected to a sampler where symbol by symbol

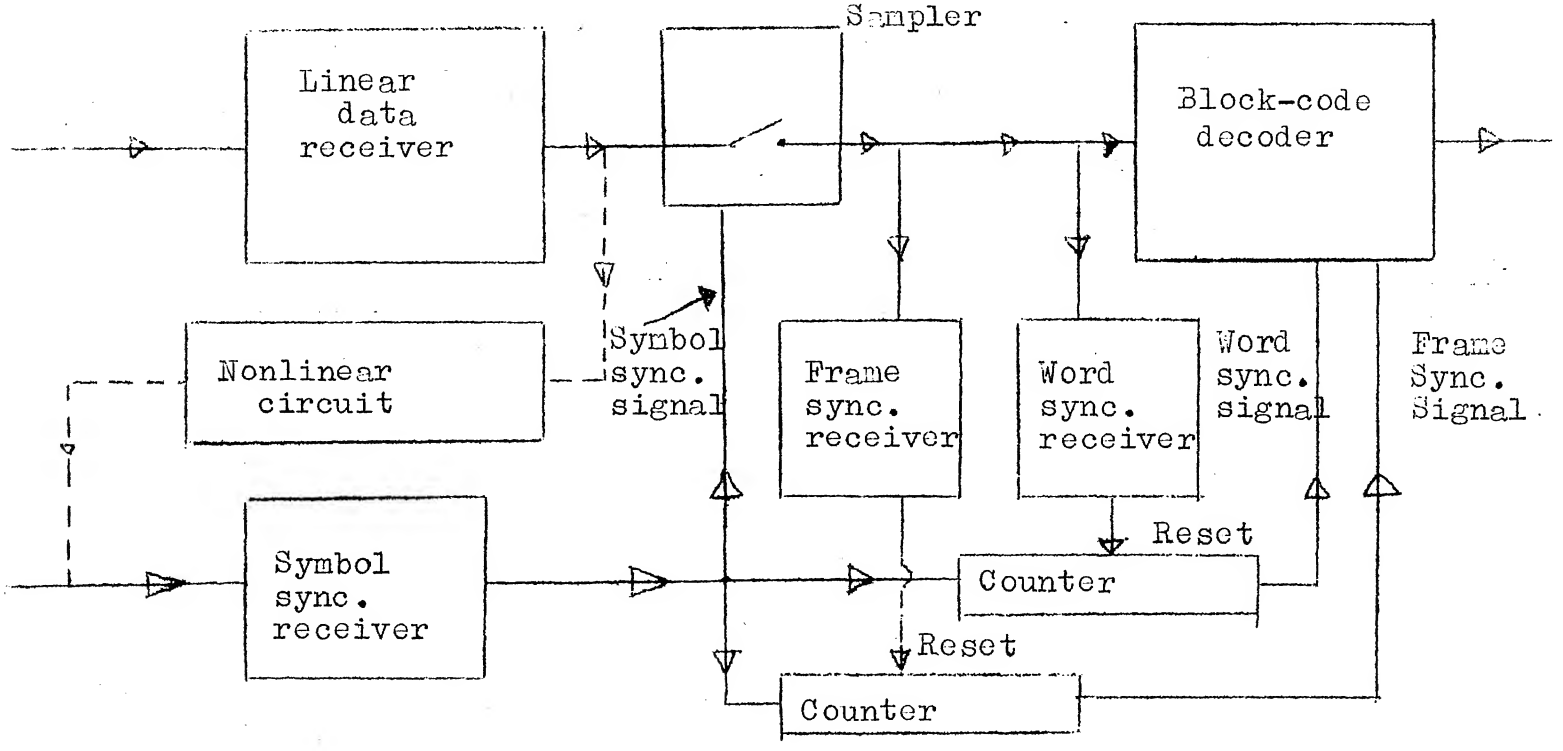


Fig. 1.1. Block diagram of conventional synchronization setup for block code decoders.

decisions are taken. The sampler requires synchronization information for its sampling instants. The symbol synchronization signal is extracted from the data itself by introducing a non-linearity in the circuit. As the duration of words and frames are multiples of the symbols, counters are used to denote the length of code words and message frames. These counters are reset by word and frame synchronization signals. The input to the counters being the synchronization signals obtained from the received data. The signals necessary for resetting the frame and word synchronous counters are obtained from the frame and word synchronous receivers which continuously scan the stream of regenerated symbols obtaine from the sampler. Special regularly inserted synchronous symbols in the data are detected by the frame and word synchronous receivers and ensure periodical reset of the counters. Although there are many variations to the receiver shown in Fig. 1.1 in general three receivers are required to receive symbol, word and frame synchronization signals.

Another method for obtaining different levels of synchronisation in block code decoders is shown in the Fig. 1.2. Here the frame synchronization receiver receives the frame synchronization signal. Since we are assuming a synchronous message structure we know that the word and symbol synchronization signal frequencies are multiple of the frame

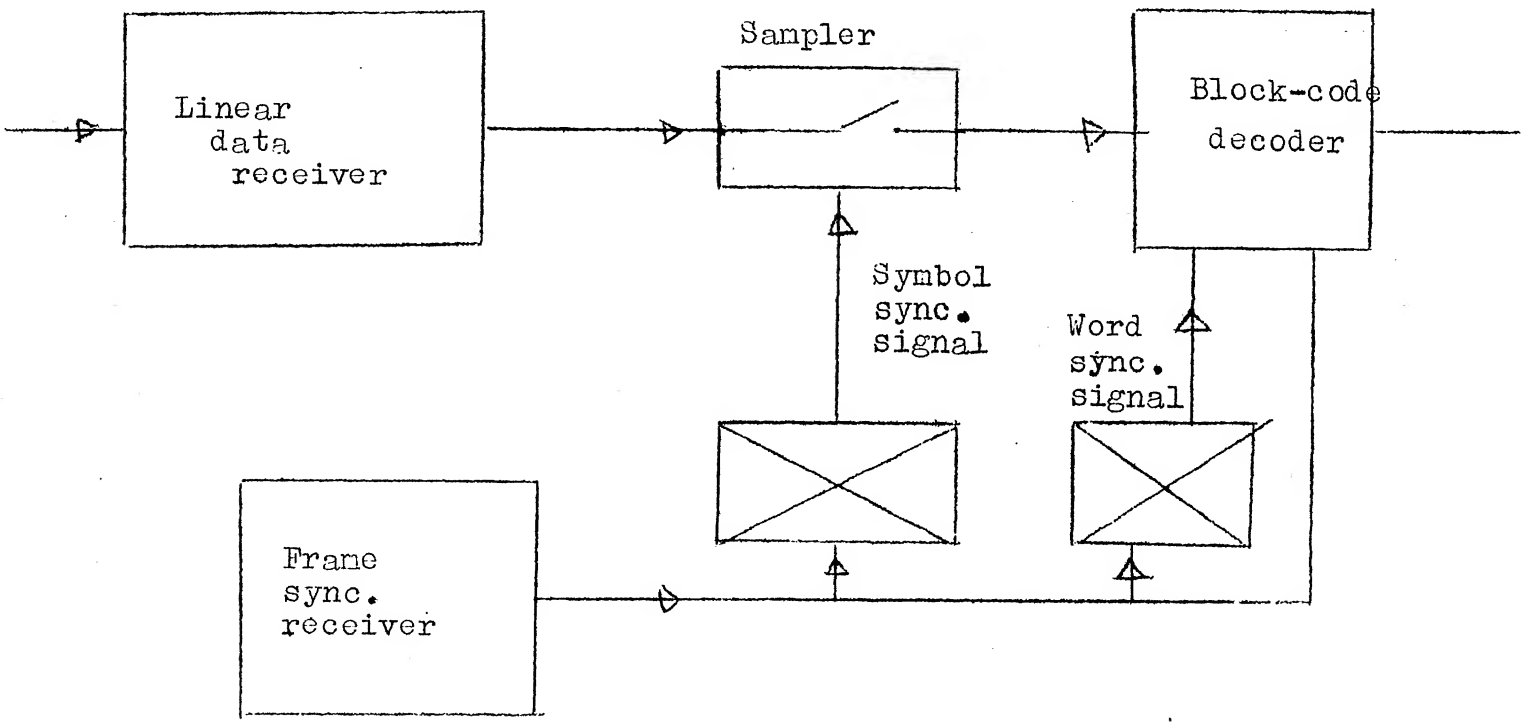


Fig. 1.2 Block diagram of simple method of synchronization of block-code decoders.

synchronization signal frequency. Hence the word and symbol synchronous clocks are derived by using two multipliers from the frame synchronization clock. As it appears this is relatively simple method of obtaining synchronization in block code decoders. The above approach is particularly useful for special periodic frame synchronization signals of a large bandwidth time product.

In chapter 2 of this thesis different methods of establishing synchronization is explained, clearly drawing the distinction between the external timing and self timing synchronization receivers. A comparison between different methods used in self timing receivers is shown in Table 2.1 of chapter 2.

Chapter 3 of this thesis deals with the considerations of how the timing deviations due to improper synchronization affects the error probability is analysed. Once the inter symbol interference is avoided by methods proposed by Nyquist the major source of error is due to the timing deviations. This has been shown both when the data is transmitted at the Nyquist rate as in an ideal system as well as when it is transmitted at a lower rate as in a practical system.

Chapter 4 contains the analysis of the phase locked loop with a sawtooth comparator, which forms the basic building block of the symbol synchronizer fabricated. Because of its linear characteristic of the phase error vs. output voltage over a wide range of $-\pi$ to $+\pi$, it offers many advantages compared to a conventional sinusoidal phase detector. Thus a sawtooth comparator is ideally selected for the symbol synchronizer.

Chapter 5 deals with the symbol synchronizer constructed. A brief description of the symbol synchronizer fabricated, along with the descriptions of some of the important components like phase detector and voltage controlled oscillator is given in this chapter.

Chapter 6 is the concluding chapter. It contains the test results showing the oscilloscope waveforms of input data signals and the synchronization waveform obtained from it. One can easily visualise the occurance of the transitions at the same instant in data waveform as well as in the synchronization signal which confirm they are in phase.

A Bibliography on synchronization is added in appendix A.

CHAPTER 2

METHODS FOR SYNCHRONISATION

Methods for synchronisation can be classified broadly into two catagories. They are external timing and self timing synchronisations.

In external timing receivers, a synchronisation signal or a pilot tone is transmitted separately alongwith the data stream. So this requires additional bandwidth for the transmission of synchronisation signal. Alternately, the same bandwidth can be utilised for transmission of both data as well as synchronisation signals. This is known as common bandwidth transmission of data and synchronisation waveforms.

Fig. 2.1 shows the block diagram for extraction of synchronisation clock signal when it is transmitted separately. Fig. 2.2 shows the timing diagram of the waveforms at different points in the block diagram. The input tuned circuit is tuned to the transmitted synchronisation frequency. The data stream doesn't appear at the output of the tuned circuit as the tuned circuit is a very narrow band resonant network. The output of the resonant circuit is shaped into a square wave by means of the limiter. The

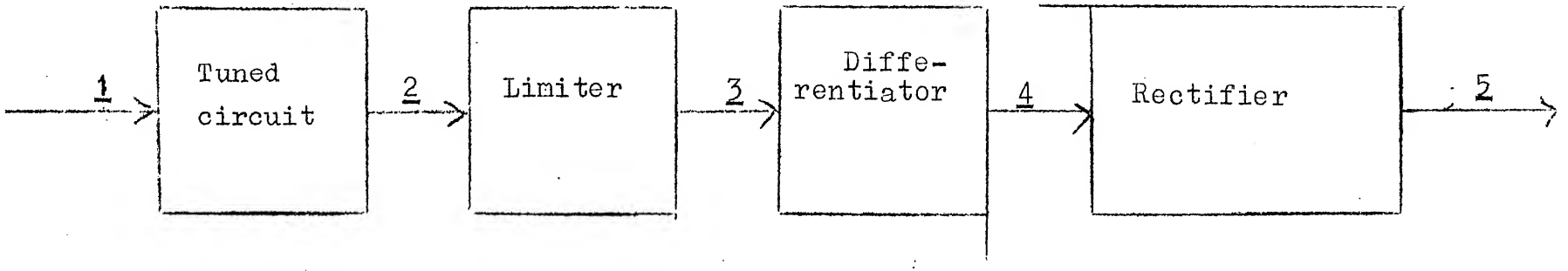


Fig. 2.1. Block diagram for recovery of seperately transmitted synchronization signal.

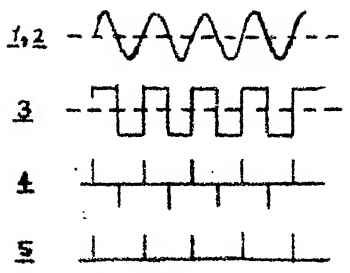


FIG. 2·2 WAVE FORMS AT DIFFERENT POINTS OF THE SYNCHRONIZATION RECEIVER SHOWN IN FIG. 2·1

square wave is then differentiated by the next block which gives the -ve and +ve going pulses. The rectifier removes the negative going pulses. Thus we obtain one +ve going pulse for every one period of the synchronisation clock frequency. These pulses are then fed to sampler for controlling the sampling instants. Since the data as well as the synchronization frequency are transmitted in the same channel they undergo the same delay etc. and hence no phase adjustment is required at the receiver. The frequency spectrum of the data signals as well as the synchronisation pilot is shown in Fig. 2.3. For good signal-to-noise ratio performance a phase locked loop can be used instead of tuned circuit shown in Fig. 2.1.

If, on the other hand the data and synchronisation signals are transmitted in the common bandwidth, the operation can be shown by a block diagram shown in Fig. 2.4. At the transmitter the data symbols and the synchronisation signal are added together by a linear adder. The synchronisation signal added to the data signal is of double the period of the clock frequency with which the data stream is generated. The amplitude of the synchronisation signal is less than half of the data signals. The data signals and the synchronisation waveform are added together in such a fashion that the transitions in the two waveforms occur at the same instants

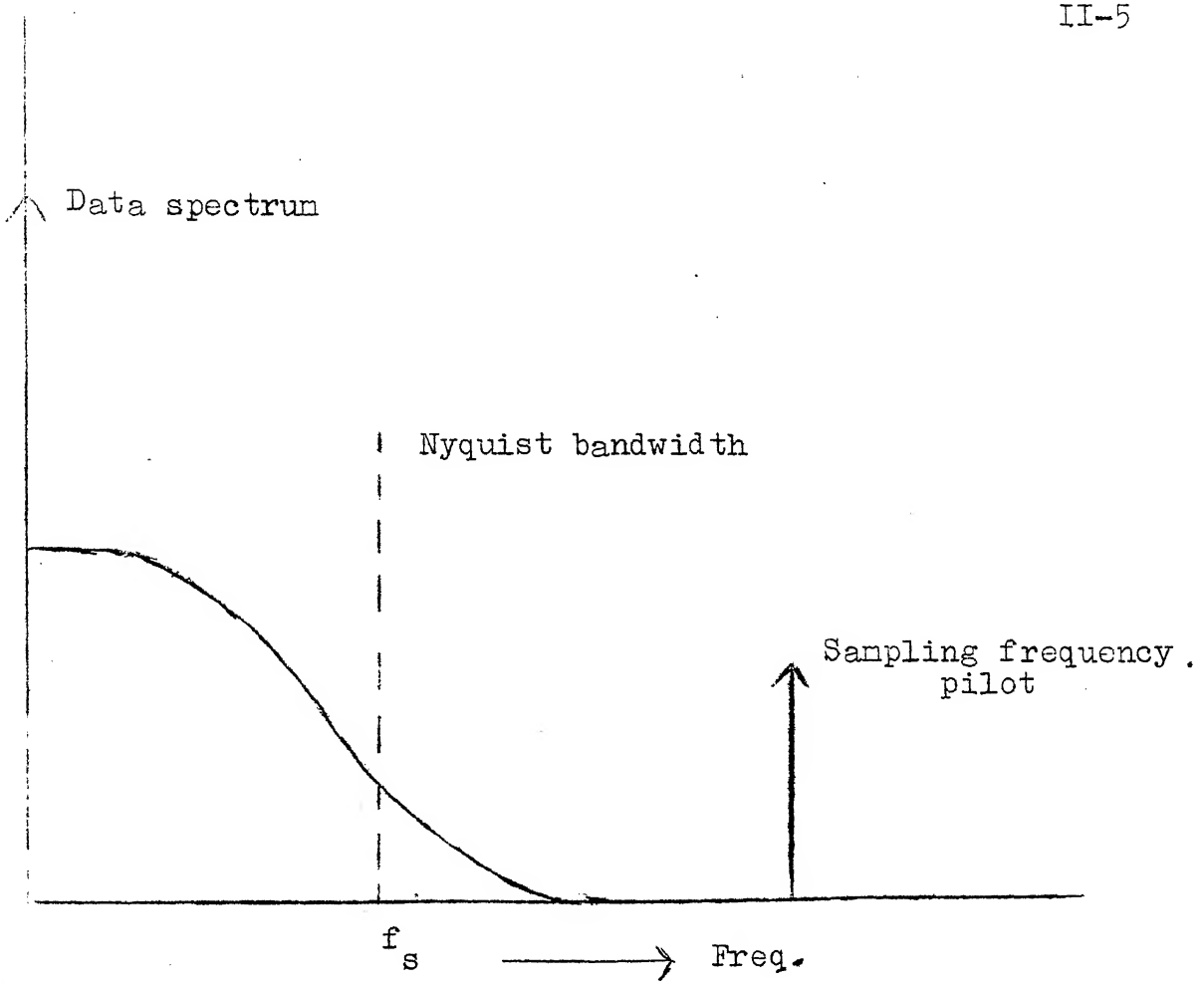


Fig. 2.3. Frequency diagram showing baseband data spectrum and the synchronization frequency pilot.

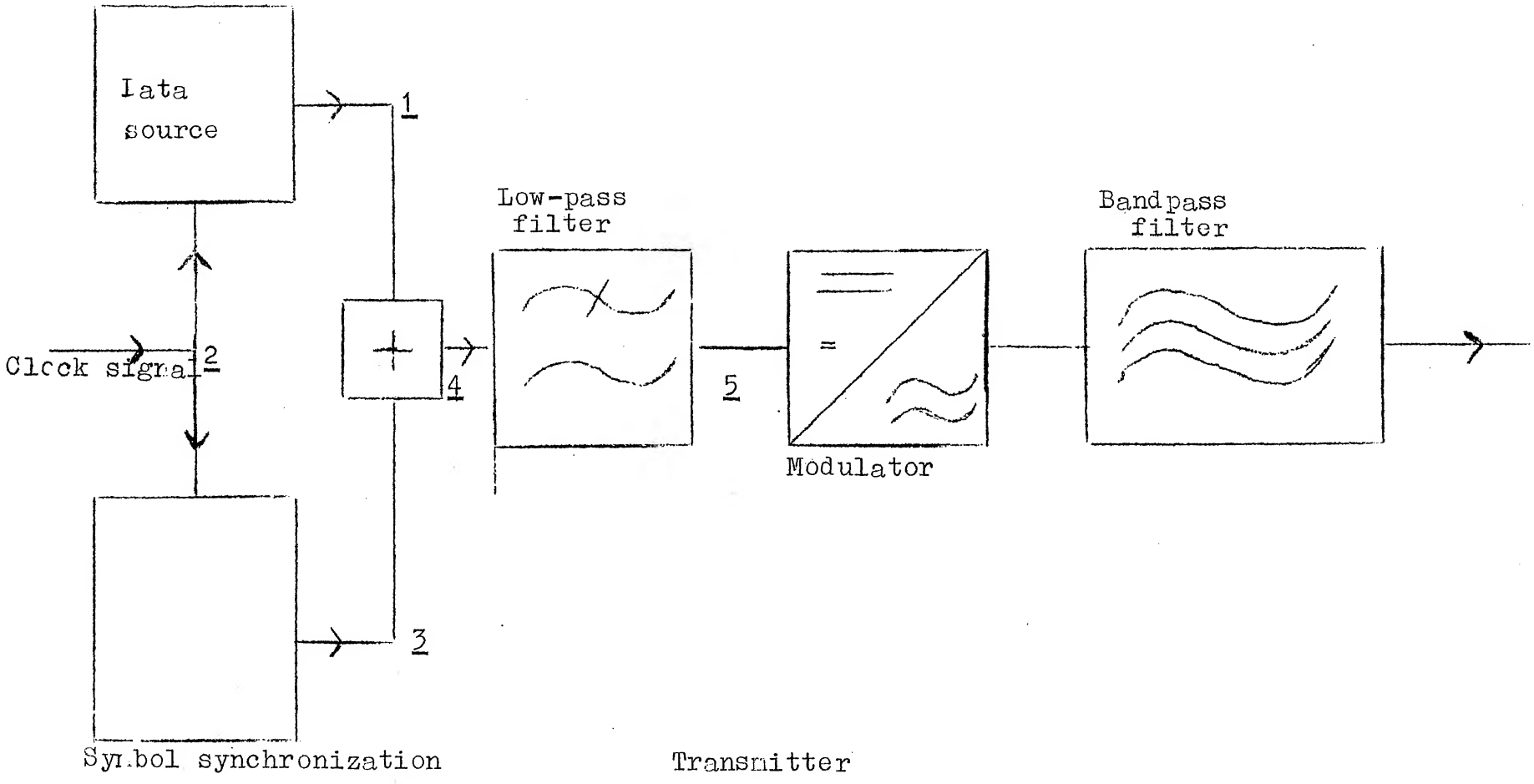
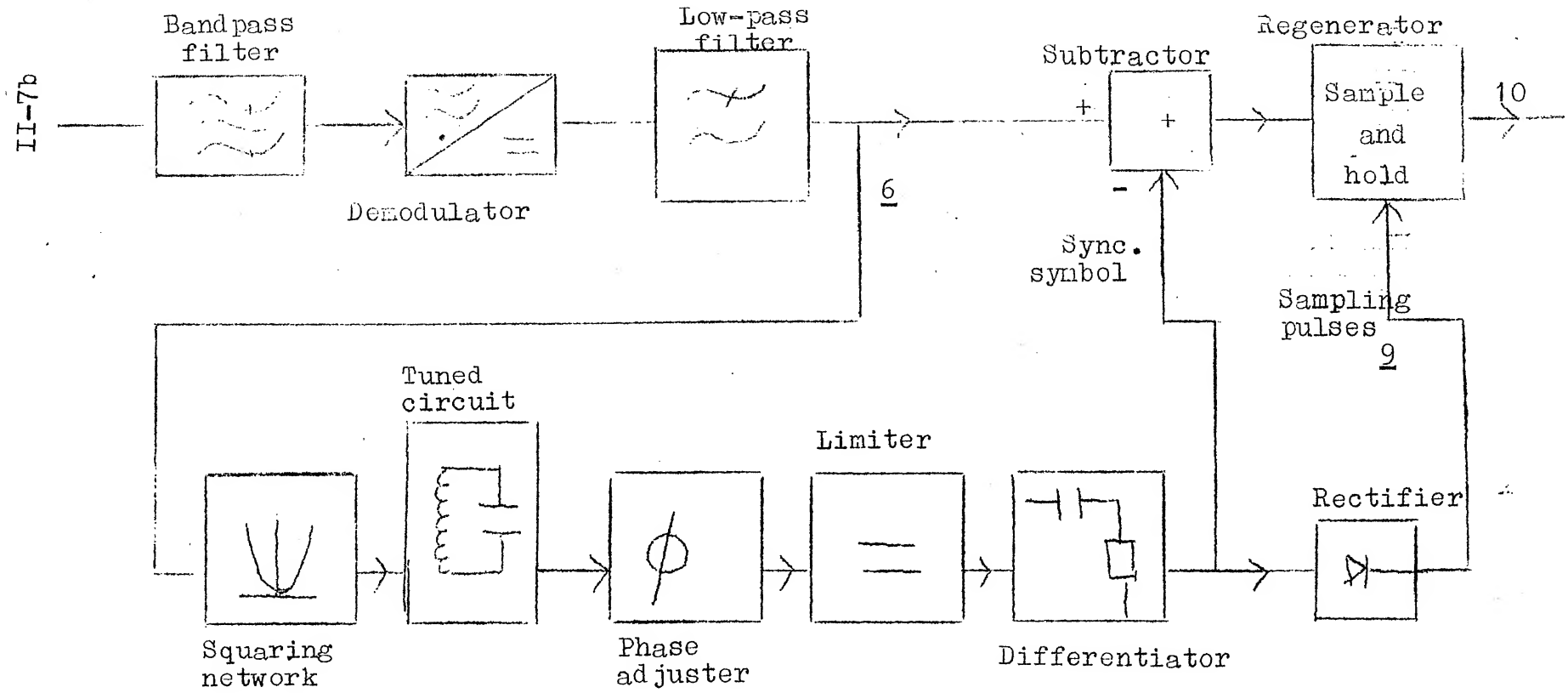


Fig. 2.4. (contd. in II-7b)



= Fig. 2.4. Block diagram of the binary data transmission systems with common bandwidth transmission of data signals and symbol synchronization waveforms.

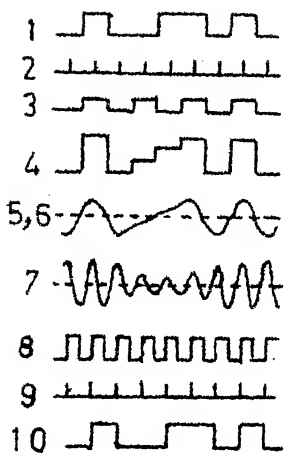


FIG. 2.5 DIAGRAM SHOWNING THE SIGNAL SHAPES AT VARIOUS POINTS NOTED IN FIG 2.4

The added signals are passed through low pass filter to smoothen out fast transitions. After modulation and band-limiting the signals are sent into the channel.

At the receiver the input stage of the synchronisation signal receiver consists of a squaring network, with a quadratic amplitude characteristic. This network will double the frequency of the synchronisation signal. The tuned circuit following the quadratic network pass the synchronisation signal rejecting the other frequency components. After proper phase adjustment, limiting, differentiation and rectification we can get the sampling pulses which are utilised to control the sampler. The synchronisation waveform will be subtracted from the baseband signal before they are fed to the sampler, since baseband signal contains both data and synchronisation waveforms.

Though this method has got the advantage of bandwidth economy it suffers from the disadvantage of interference due to the synchronisation signal present in the same bandwidth.

Self Timing Systems:

Basically there are four methods by means of which digit synchronisation can be established by means of self

timing technique. These are direct resetting, selected resetting, incremental adjustment, and phase locked loop.

In the direct resetting technique now obsolete, every edge of the incoming data pulse is used to correct the receiver clock, there by adjusting the phase of the receiver synchronisation clock.

In the selected resetting technique also obsolete now, the digit rate clock (the symbol synchronisation clock) is reset only when a out of phase condition between the data stream and the digit rate clock is indicated by an indicator.

The incremental adjustment technique utilises a digital phase locked loop with a oscillator whose frequency is much higher than the digit rate clock. Pulses are added or deleted to the oscillator output depending on the incoming data symbols, so as to maintain synchronism with the oscillator output, divided down to the digit rate clock frequency and the data stream. A block diagram of the system is shown in Fig. 2.6. Let us consider a two phase clock whose frequency is 64 times greater than the bit timing waveform frequency. The output of the two phase clock is divided by binary counter of ratio 64:1 to obtain the bit timing. The transitions in the incoming data stream are detected by the transitions detector or a zero crossing detector. The output of the

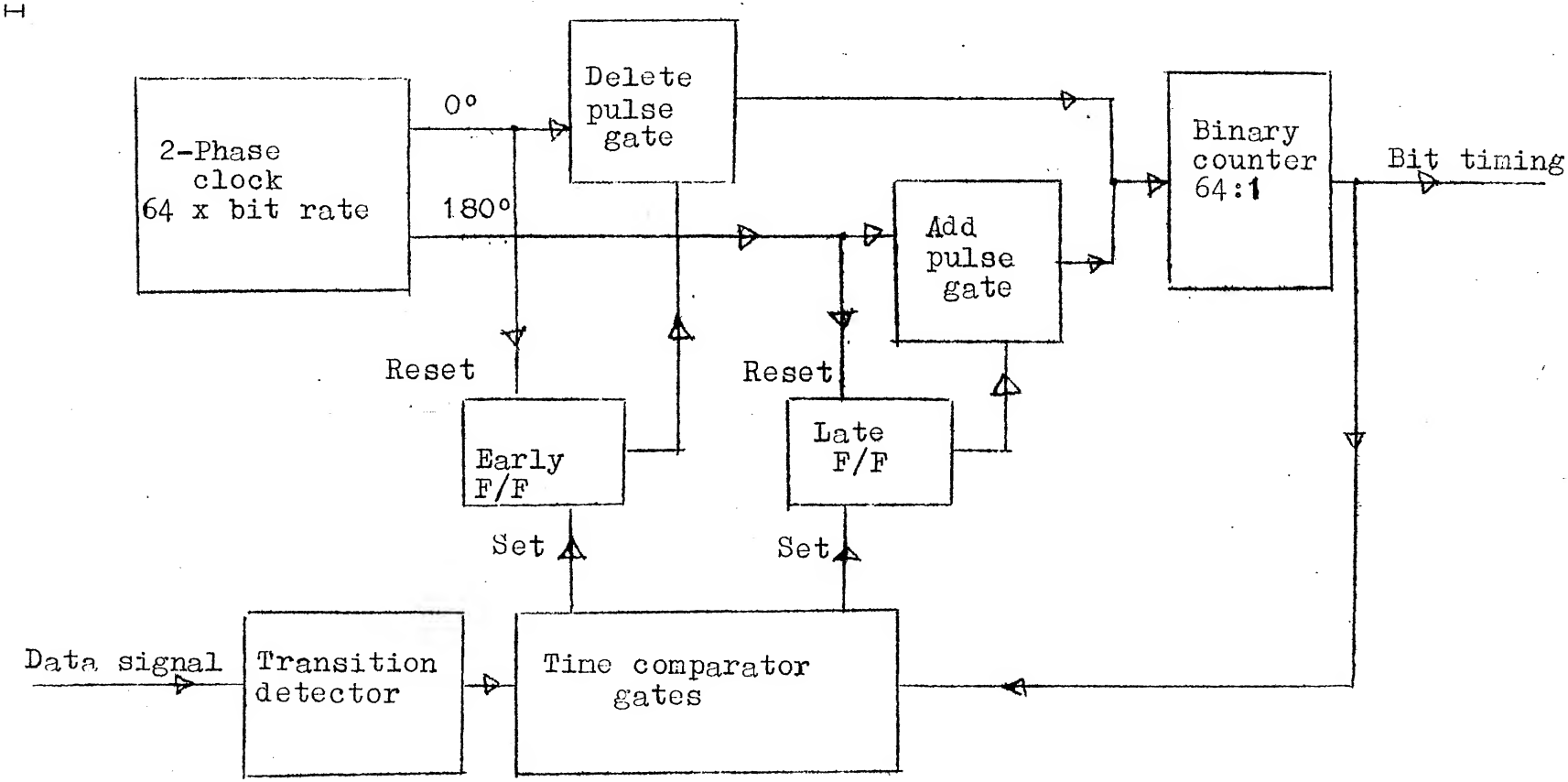


Fig. 2.6 Block diagram of incremental adjustment symbol synchronizer.

transition detector is compared with that of the bit timing signals with the help of the time comparator gates. If the phase of bit timing signal leads that of the incoming data the early flip-flop is set which in turn activate the delete pulse gate which deletes one of the counting pulses of the two phase clock from reaching the counter and hence output of the counter will be made to lag in phase by $\frac{1}{64}$th of the bit interval. On the other hand if the bit timing signal lags in phase the late flip-flop will be set which in turn activates the add pulse gate, which adds an additional pulse to the two phase clock pulses and hence the output of the counter will be made to lead in phase by $\frac{1}{64}$th of the bit interval. To obtain highest degree of accuracy it is desirable to provide some kind of memory to the system so that when the input data stream is absent the phase of the bit timing signals will remain in the last setting.

The phase locked loop techniqueinvolves the comparison of the frequency of the incoming data stream with that of a local oscillator and the error is utilised for correction of the frequency and phase of the local oscillator. The technique is explained in detail subsequently.

The performance characteristics of the various self timing systems are compared in table 2.1, with respect

to noise and jitter immunity, accuracy and stability.

Table 2.1 Self Timing digit Synchronisers Comparison

Technique	Direct reset	Selected reset	Incremental	Phase locked loop
Immunity to noise	Poor			Excellent
Immunity to jitter	Poor			Excellent
Accuracy	Acceptable			Excellent
Stability	Good			Excellent
Complexity	Low	Medium	Medium	Medium

Table 2.1 tells us about the selection of a particular technique depending on the accuracy required. When a highly accurate digit synchronisation is needed we have to go for phase locked loop technique.

Comparison of External and Self timing Systems:

No doubt an accurate timing for digit synchronisation is provided by separate transmission of clock signals. But the external timing system suffers from the following disadvantages.

1. It is not economical since we are utilising additional bandwidth for the transmission of clock.

2. The transmission of additional signal is redundant because the necessary timing signal can be extracted from the signal transition in the data signals.

3. Processing of the data signals has to be abandoned if the synchronisation signal has been lost by chance even after receiving the data signals.

4. It is vulnerable to jamming, which is very important in defence communications.

Also, because of the recent developments in cheap and fast I.C.'s have made the synchronisation with the help of common bandwidth signals feasible. And hence, we shall confine our discussion to the self timing systems only.

CHAPTER 3

CONSIDERATION OF PROBABILITY OF ERROR VS. TIME JITTER

The errors in binary data transmission manifested due to the additive gaussian noise, inter symbol interference and timing in-accuracies. The inter symbol interference can be eliminated using simply the methods suggested by Nyquist. But in the presence of timing inaccuracies inter symbol interference plays a vital role, thus an accurate timing information is necessary to the sampler in order to keep the error probability within tolerable limits. We study the above facts with reference to binary data transmission.

The block diagram of the binary antipodal data transmission system is shown in the Fig. 3.1. It consists of a bivalent source which generates the bivalent messages. The coder, converts the bivalent messages into an appropriate waveform. Here we are especially interested in the synchronous message structure, which means the successive messages are transmitted at regular intervals of T_o.

Let us assume that transmission channel is band limited to the bandwidth $(-w_d, + w_d)$ and the additive noise to be Guassian with zero mean and band limited to the available bandwidth $(-w_d, + w_d)$.

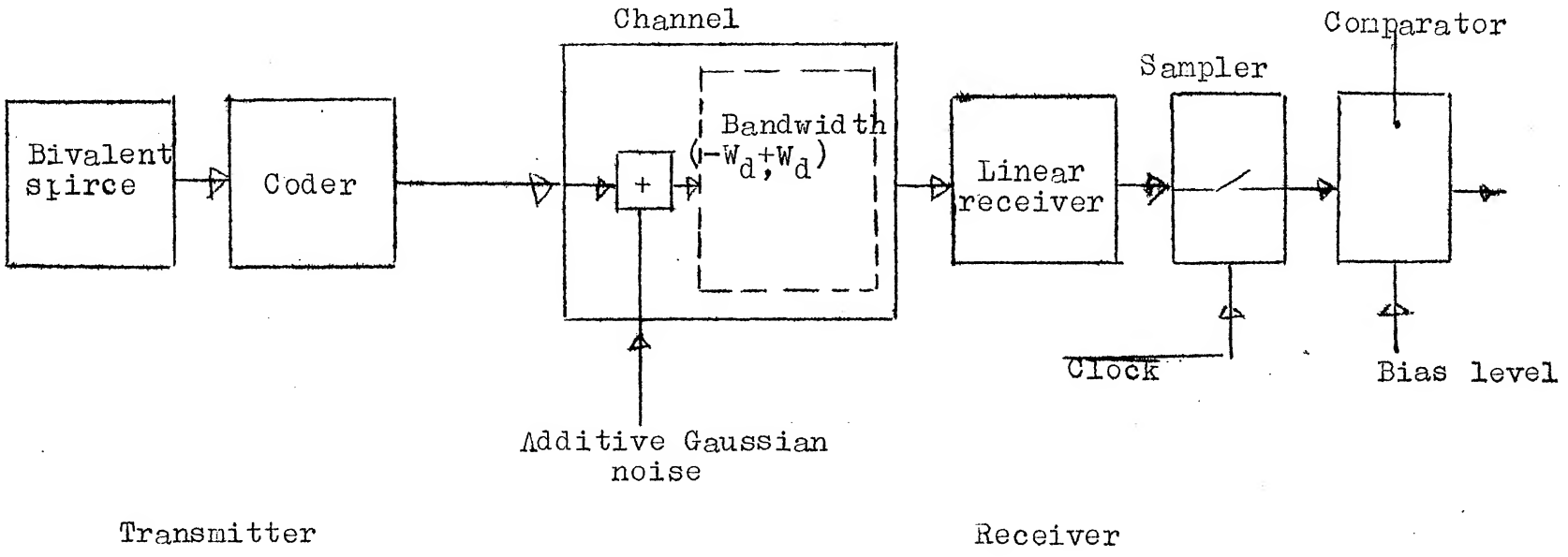


Fig. 3.1 . Block diagram of binary antipodal data transmission system.

Let us restrict our discussion to a linear receiver connected to a sampler as shown in the Fig. 3.1. The sampler takes the samples at every T_o seconds and the samples are compared with a fixed bias level to arrive at decisions.

Let us now study the dependence of the average error probability on intersymbol interference, noise and timing deviations of the sampling instants for this type of receiver. Let us also discuss some possible ways of minimising the average decoding error probability.

Let us denote the Kth received waveform by $a_k\, r(t-t_k)$ where $a_k=1$ or -1 while $t_k=K\, T_o$ is the nominal decision time for the waveform considered and energy contained in $r(t)$ be E.

Let the receiver response to $r(t)$ with a fourier transform $G_r(f)$, is given by

$$y(t)=\int_{-\infty}^{+\infty} G_r(f)H(f)\, \exp(2\pi jft)df, \qquad (3.1)$$

where $H(f)$ is the transfer function of the linear receiver. In the absence of noise the receiver response to the mth waveform may be written as

$$a_m y(t-mT_o)=a_m \int_{-\infty}^{+\infty} G_r(f)H(f)\exp 2\ \ jf(t-mT_o)\, df. \qquad (3.2)$$

At the instant t_k the response of the receiver to the mth waveform equals $a_m y(t_k-mT_o)$. Let us assume that the

intersymbol interference extends over N symbols preceding and N symbols following the time t_k considered, which is the time of detection of the kth message waveform. Thus the response of the linear receiver at time t_k becomes

$$Y(i,t_k) = \sum_{m=k-N}^{k+N} a_m(i)y(t_k - mT_o), \qquad (3.3)$$

where i stands for one of the possible 2^{2n+1} sequences that can be constructed with 2N+1 binary message waveforms. Further for a small deviation δ of the decision instant t_k the output of the sampler in the absence of noise is given by

$$Y(i,t_k-\delta) = \sum_{m=k-N}^{k+N} a_m(i)y(t_k - mT_o - \delta). \qquad (3.4)$$

It can be seen that the inverse of a particular sequence of 2N+1 successive waveforms gives a response at the sampler input of the same magnitude but of opposite sign. If the inverse of the ith sequence is denoted by $\bar{i}$, so

$$\bar{i} = 2^{2N+1} + 1 - i \text{ for } i = 1, 2, \ldots, 2^{2N}$$

and

$$a_m(\bar{i}) = -a_m(i) \text{ for } m = k-N, k-N+1, \ldots, k+N-1, k+N; a_k(i) = 1,$$

then we have

$$Y(i,t_k-\delta) = -Y(\bar{i},t_k-\delta) \qquad (3.5)$$

The apriori probabilities of occurance of the ith and $\bar{i}$th sequences will be denoted by $P_r(i)$ and $P_r(\bar{i})$ respectively

Let us assume that $P_r(i)=P_r(\bar{i})$ for any i.

In the presence of transmission noise the output of the sampler for any ith and $\bar{i}$th sequence at the instant $t_k-\delta$ is given by $x(t_k-\delta)$. If $\hat{a}_k$ denotes the decoder output for the decision instant considered, the below mentioned decision rule can then be applied at time $t_k-\delta$.

$$\hat{a}_k=1 \text{ if } x(t_k-\delta)>0,$$
$$\hat{a}_k=-1 \text{ if } x(t_k-\delta)<0. \qquad (3.6)$$

It is required that $Y(i,t_k)>0, \qquad (3.7)$

as this implies an error free decision for any i or $\bar{i}$ in the absence of noise and sampling inaccuracy. For the noise spectral density $S_n(f)$ assumed the noise output of the receiver is given by

$$\sigma_n^2 = \int_{-\infty}^{+\infty} S_n(f)\,|H(f)|^2\,df. \qquad (3.8)$$

The probability of decoding error for any ith sequence and kth message waveform is equal to the probability of the noise contribution of the sample at $t_k-\delta$ has an amplitude in the range from $-\infty$ to $-Y(i,t_k-\delta)$. Therefore we can write

$$P_e(i,\delta) = \frac{P_r(i)}{\sigma_n(2\pi)^{1/2}} \int_{-\infty}^{-Y(i,t_k-\delta)} \exp(-v^2/2\sigma_n^2)\,dv. \qquad (3.9)$$

Therefore the decoding error probability for $\bar{i}$th sequence and kth message waveform in given by

$$P_e(\bar{i},\delta) = \frac{P_r(\bar{i})}{\sigma_n(2\pi)^{1/2}} \int_{-Y(\bar{i},t_k-\delta)}^{\infty} \exp(-v^2/2\sigma_n^2)dv. \quad (3.10)$$

for $P_r(i) = P_r(\bar{i}) = 2^{-(2N+1)}$ it is easy to see that $P_e(i,\delta) = P_e(\bar{i},\delta)$. Then the average probability of error decoding is given by

$$\bar{P}_e = 2^{-(2N+1)} \int_{-\infty}^{+\infty} P_\delta(\delta)d\delta \sum_{i=1}^{2^{2N}} P_e(i,\delta) + P_e(\bar{i},\delta) \quad (3.11)$$

Where $P_\delta(\delta)$ denotes the probability density function of the sampling inaccuracy. We know the error function is defined as

$$\operatorname{erfc}(a) = \frac{2}{\sqrt{\pi}} \int_a^{\infty} e^{-v^2} dv, \quad (3.12)$$

Therefore

$$\bar{P}_e = 2^{-(2N+1)} \int_{-\infty}^{+\infty} P_\delta(\delta)d\delta \sum_{i=1}^{2^{2N}} \operatorname{erfc} \frac{Y(i,t_k-\delta)}{\sigma_n\sqrt{2}} . \quad (3.13)$$

Eventhough the above formula is derived for the kth decision instant it is the general relationship between the average error probability and perturbations due to noise, intersymbol interference and sampling inaccuracies.

At this stage let us find out the possible methods of implementation of a optimum decoder. Let us first try to

minimise $\bar{P}_e$ and determine the corresponding receiver characteristic H(f) for a given r(t) i.e. the message waveform.

A suitable approach may be based on the fact that the intersymbol interference can be made negligible at equidistant decision instants by methods proposed by Nyquist. This approach is based on the following identity.

$$\frac{1}{T_o} \sum_{n=-\infty}^{+\infty} G_y(f + \frac{n}{T_o}) = \sum_{n=-\infty}^{+\infty} y(nT_o)\exp(-2\pi jfnT_o), \tag{3.14}$$

$G_y(f)$ denotes the fourier transform of y(t). If we require $y(nT_o) = 0, n = \pm 1, \pm 2\ldots$, From (3.1)

$$y(0) = \int_{-\infty}^{+\infty} G_r(f)H(f)df, \tag{3.15}$$

then this implies that the intersymbol interference vanishes at decision instants which are a time T_o apart. Therefore condition (3.14) then requires

$$\sum_{n=-\infty}^{\infty} G_y(f + \frac{n}{T_o}) = y(0)T_o \tag{3.16}$$

A special but unrelizable situation is given by

$$G_y(f) = y(0)T_o, \quad -\frac{1}{2T_o} \leq f \leq \frac{1}{2T_o} \tag{3.17}$$

which specifies the minimum bandwidth required at the Nyquist symbol rate $\frac{1}{T_o}$. Therefore $w_d = \frac{1}{2T_o}$ where w_d is the

Nyquist bandwidth. When $w_d > \frac{1}{2T_o}$ many possible designs of $G_y(f)$ can be obtained which satisfy (3.16), but at a transmission rate below the Nyquist symbol rate. We know that the effect of Guassian noise can be minimised using a matched filter or a correlator receiver in the absence of intersymbol interference.

Let us consider a matched filter receiver. The message waveform received is r(t) and its ftransform be $G_r(f)$. Then the ideal matched filter transfer function is $\varrho\ G_r^*(f)$ where ϱ is a factor of value unity and $G_r^*(f)$ is the complex conjugate of $G_r(f)$. Now the spectrum of the message contribution y(t) at the output of the matched filter may be written as

$$G_y(f)=\varrho\, G_r(f)\ G_r^*(f)=\varrho\left|G_r(f)\right|^2. \qquad (3.18)$$

From (3.1)

$$y(0)=\varrho\int_{-\infty}^{+\infty} G_r(f)G_r^*(f)df=\varrho\, E. \qquad (3.19)$$

To satisfy (3.16) it follows that

$$\sum_{n=-\infty}^{+\infty}\left|G_r\left(f+\frac{n}{T_o}\right)\right|^2=ET_o. \qquad (3.20)$$

Thus we can find a message waveform r(t) that corresponds to the fourier transform $G_r(f)$ which obeys (3.20). This is illustrated by the plots in Figs. 3.2 to 3.3.

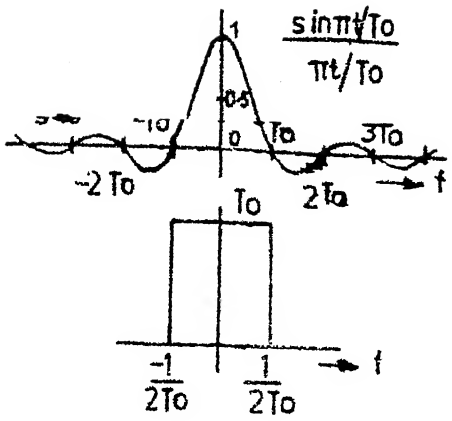


FIG.3.2 IMPULSE RESPONSE OF A IDEAL LOW PASS FILTER AND ITS FOURIER TRANSFORM

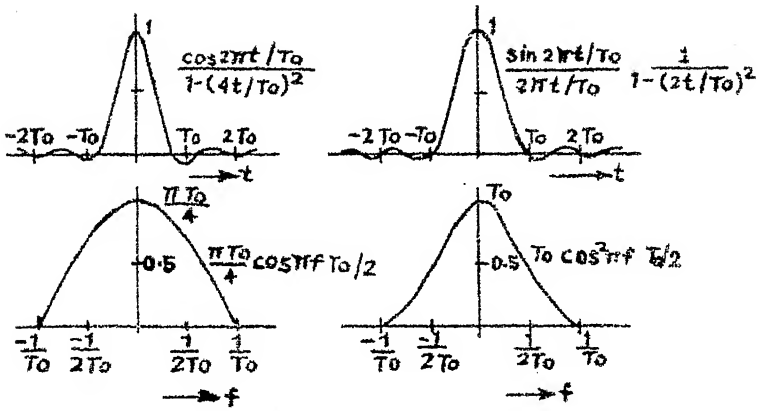


FIG.3.3. DATA WAVE FORMS AND THEIR FOURIER TRANSFORMS

The ideal case of transmission at Nyquist rate is given by

$$r(t)= \left(\frac{E}{T_o}\right)^{1/2} \frac{\sin(\pi t/T_o}{\pi t/T_o} \; ; \; y(t) = \varrho E \frac{\sin(\pi t/T_o)}{\pi t/T_o} \tag{3.21}$$

$$G_r(f)=\begin{cases}(ET_o)1/2, & f \leq 1/2T_o \\ 0 & f > 1/2T_o\end{cases} ; \; G_y(f)=\varrho \left|G_r(f)\right|^2$$

$$\begin{cases}ET_o, & f \leq 1/2T_o \\ 0 & f > 1/2T_o\end{cases} .$$

Another practical example is that r(t) and y(t) quickly decay to zero but needs twice the Nyquist bandwidth is given by

$$r(t) = \frac{4}{\pi} \left(\frac{E}{T_o}\right)^{1/2} \frac{\cos(2\pi t/T_o)}{1-(4t/T_o)^2} ;$$

$$y(t) = \frac{\sin(2\pi t/T_o)}{2(\pi t/T_o)} \frac{\varrho E}{1-(2t/T_o)^2} ,$$

$$G_r(f)= \begin{cases}(ET_o)^{1/2} \cos(\pi f T_o/2), & |f| \leq 1/T_o \\ 0 , & |f| > 1/T_o\end{cases} ; \tag{3.22}$$

$$G_y(f)=\varrho \left|G_r(f)\right|^2 = \begin{cases}\varrho ET_o \cos^2(\pi f T_o/2), & f \leq 1/T_o \\ 0 , & f > 1/T_o\end{cases}$$

The performance of the linear receiver can be determined by the evaluation of (3.13). When the receiver response y(t) satisfies the Nyquist condition (3.16) while $P_\delta(\delta)$ is given by a Dirac delta function at $\delta = 0$, the formula (3.16) can be reduced to

$$\bar{P}_e = 2^{-(2N+1)} \sum_{i=1}^{2^{2N}} \operatorname{erfc} \frac{a_k(i)y(0)}{\sigma_n\sqrt{2}} = \frac{1}{2}\operatorname{erfc}\left\{\frac{y(0)}{\sigma_n\sqrt{2}}\right\} \tag{3.23}$$

When the receiver filter is matched we know that $y(0) = \rho E$. For white Gaussian channel noise of spectral density $S_n(f) = \frac{N_d}{2}$ formula (3.8) shows that $\sigma_n^2 = \rho^2 N_d E/2$ Thus for an ideally matched filter and zero intersymbol interference $\bar{P}_e = \frac{1}{2}\operatorname{erfc}\sqrt{\frac{E}{N_d}}$, which is also the optimum error probability for binary antipodal data transmission.

When the sampling is inaccurate intersymbol interference plays a significant role eventhough Nyquist criterion is met. To get an insight into this effect the performance of matched filter has been analysed by ZEGERS assuming a Guassian probability density function with a zero mean and a variance which is a small fraction ϵ of T_o for the timing deviations. Thus the formula(3.16) has been evaluated for examples provided in (3.21) and (3.22). Example (3.21) provides the

the instructive insight for the limiting case of data transmission at Nyquist rate, eventhough it is not physically realizable. This situation is plotted in Fig. 3.4 where average error rate $\bar{P}_e$ is given as a function of signal to noise ratio E/N_d with N=3 and ϵ as parameter. For $N \rightarrow \infty$ the summation in (3.16) is not convergent and hence the summation is valid only for finite values of N. From the curves we can infer that the sampling jitter causes a threshold effect. The performance in the prescence of sampling jitter is quite good in the case of the other example provided by (3.22), but at the cost of twice the Nyquist bandwidth. These curves are plotted in Fig. 3.5, in which the effect of sampling jitter is clearly noticed.

We will conclude this chapter by stating that sampling jitter can have serious effects on the performance of binary data transmission systems. Thus jitter free accurate synchronisation is necessary in synchronous data communication systems.

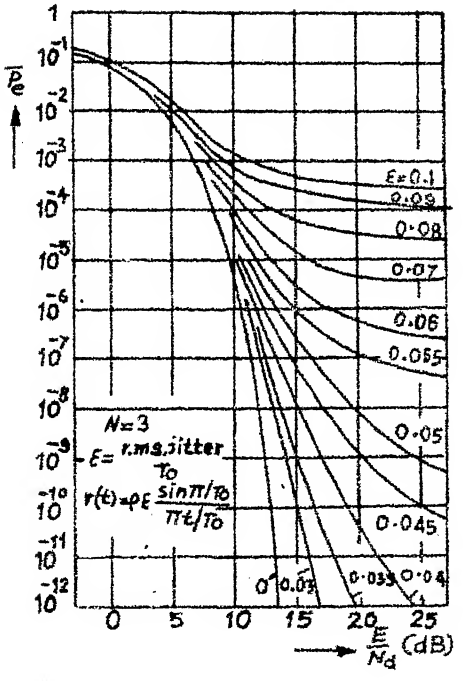


FIG.3.4 AVERAGE ERROR PROBABILITY IN BINARY ANTIPODAL DATA TRANSMISSION AT NYQUIST RATE AS A FUNCTION OF SIGNAL-TO NOISE RATIO AND ε AS PARAMETRE

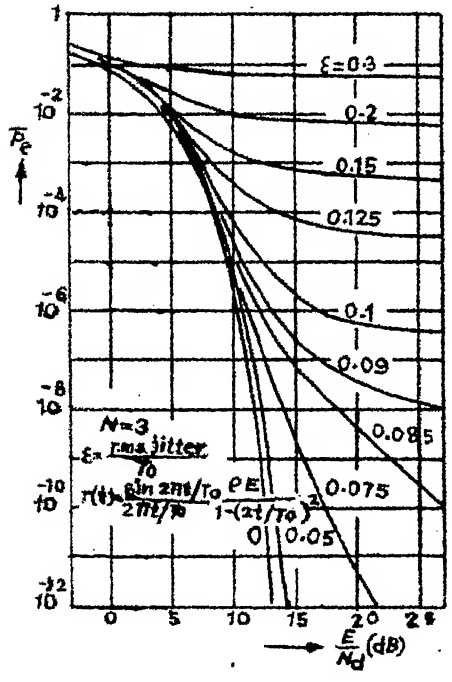


FIG.3.5 AVERAGE ERROR PROBABILITY IN BINARY ANTIPODAL DATA TRANSMISSION AT NYQUIST RATE AS A FUNCTION OF SIGNAL TO NOISE RATIO AND ε AS PARAMETRE

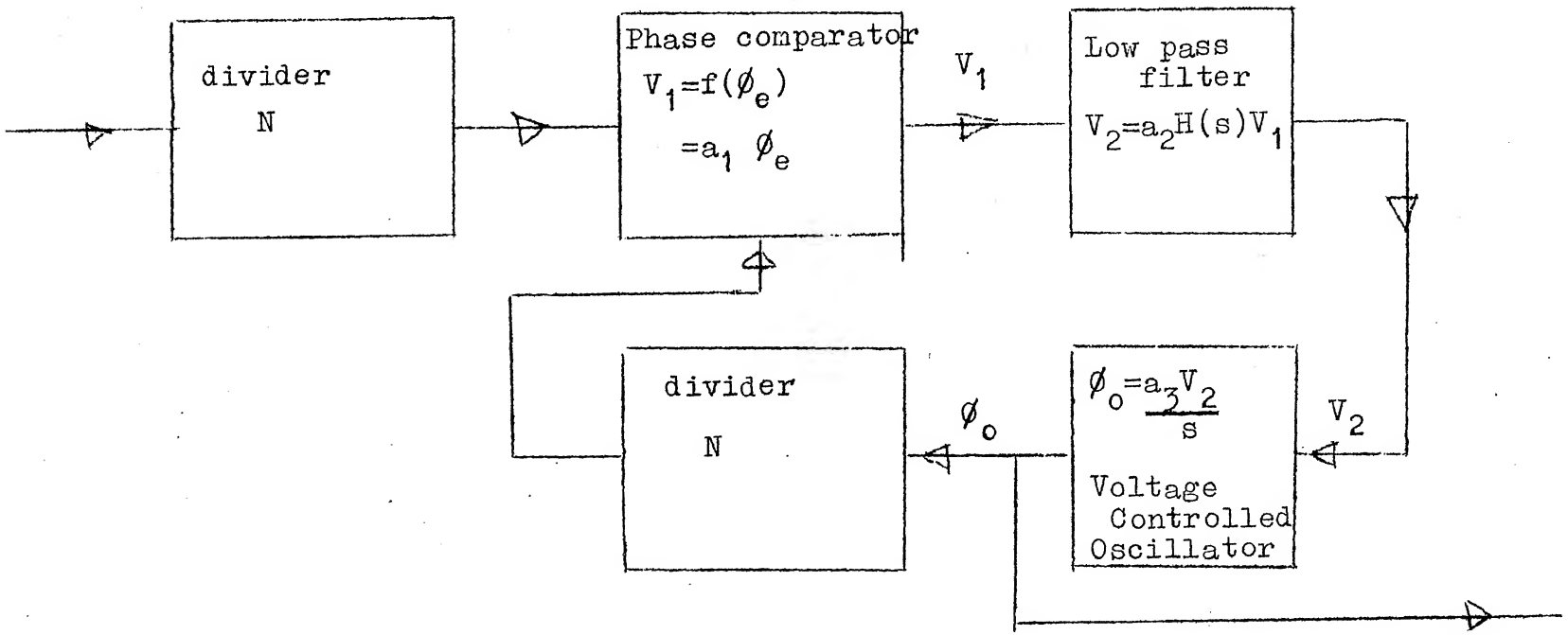
CHAPTER 4

ANALYSIS OF PHASE LOCKED LOOP WITH A SAWTOOTH COMPARATOR

The phase locked loop is known since 1930. But its widespread use is only recent with the advent of sophisticated communication fields like space communications etc. A phase locked loop is almost indespensible whenever an exact phase or frequency information is required. Thus it has got many applications in fields like communications, controls and instrumentation.

A phase locked loop produces an output frequency, depending on the phase and frequency of the input signal. Here we consider the phase locked loop using a saw-tooth comparator,which is superior to sine wave comparator because of its linear characterstic of the output voltage Vs. phase. We will observe in the next chapter that this phase locked loop with the sawtooth comparator is going to be the basic building block of the symbol synchroniser.

The block diagram of the phase locked loop is shown in the Fig. 4.1 which resembles a servo loop or a feed back amplifier. It consists of number of basic building blocks like phase comparator, low pass filter, voltage controlled



$\phi_e=\phi_i-\phi_o$, U = Forward gain of the loop

$$= \frac{a_1\ a_2\ a_3}{s}\ H(s) = \frac{a}{s}\ H(s)$$

Fig. 4.1. Block diagram of the Phase Locked Loop.

oscillator and frequency dividers.

Frequency dividers:

There are two frequency dividers in the circuit, one in the forward path and the other in the feedback path. These dividers divide the frequencies of the incoming signal as well as the voltage controlled oscillator's frequency, in such a way that the signals of the same submultiples are applied to the input terminals of the phase comparator. These dividers infact extend the range of the comparator. The probability of discontinuity due to large fluctuations in frequency diminishes as the division ratio increases. It also reduces the over all loop gain, a reduction in jitter in the signal supplied to the comparator and allows the comparator to operate at a lower frequency.

Phase comparator:

The phase comparator is the error detector in the loop. It compares the phase of the input and output signals and generates the voltage depending on the phase difference. It cannot differentiate between different cycles of input and output submultiples. Therefore its output is a periodic function of the phase difference between the input and output submultiples. The period of the output waveform of the comparator is equal to one cycle of the submultiple frequency

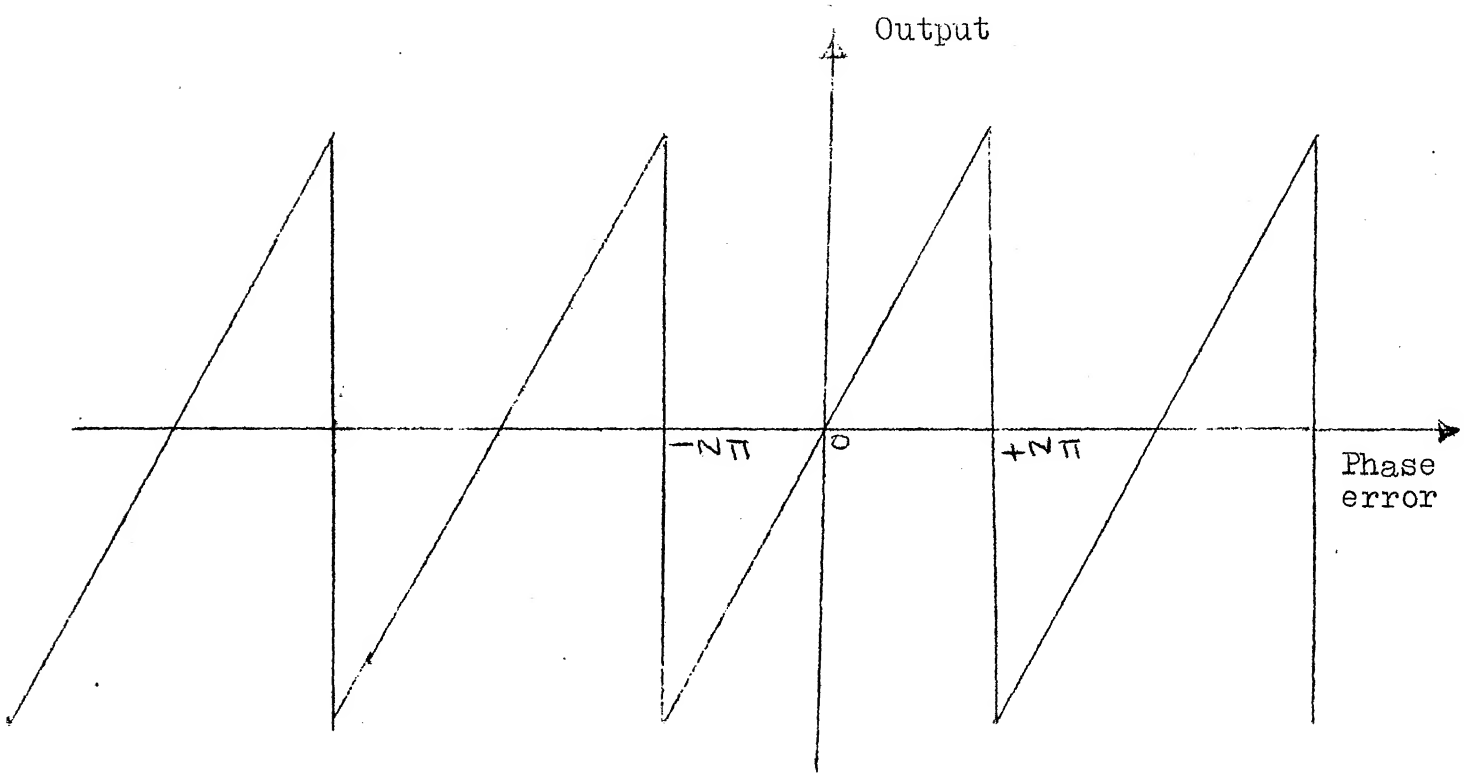


Fig. 4.2. Phase error vs. output voltage characteristic of a sawtooth comparator.

The characteristic of the sawtooth comparator is shown in Fig. 4.2, as we are interested in analysing the loop using a sawtooth comparator.

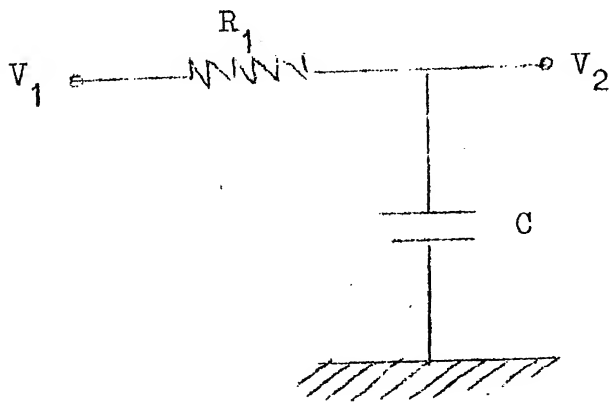
The range of the comparator in terms of the cycles of input and output frequency can be increased by increasing the dividing ratio. The linear portion of this range is important because the longer it is the smaller is the distortion. In addition it also improves the noise threshold, pull in range and hold in range.

Loop filter:

The loop filter is a low pass filter which attenuates fast changes in the output of the phase detector caused by noise and high frequency components in the output of the phase comparator. It can be a simple R-C filter or a lead lag filter as shown in Fig. 4.3.

Voltage control oscillator:

The voltage controlled oscillator is used to generate the output signal of the required phase. Phase is the integral of the frequency and therefore the oscillator acts like a perfect integrator since it has got long time constant and memory. The characteristics of the voltage control oscillator required for the communication signal are: a good



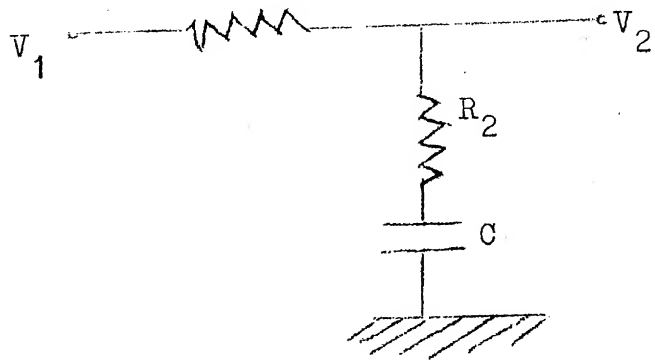
$T_1 = R_1 C$

$_1 = a\, R_1 C$

$_2 = 0$

$H(s) = \frac{1}{1+sT_1}$

a) R-C filter



$T_1 = (R_1+R_2)C$

$_1 = a(R_1+R_2)C$

$_2 = R_2\, C$

$_2 = aR_2\, C$

$H(s) = \frac{1+sT_2}{1+sT_1}$

b) lead lag filter

Fig. 4.3 . Low pass filter

phase stability, a linear frequency/control voltage characterstic and a large gain factor.

Aligned operation of the loop:

Let us assume that the input frequency is equal to the output frequency. Then there is no error voltage from the phase detector. If we advance the phase of the incoming signal the phase detector output gives rise to an error signal which advances the phase of the voltage controlled oscillator. The circuit cannot settle down until the phase of the output is equal to the phase of the input.

Mistuning:

Assume that the input frequency is slightly grater than the output frequency, so that the input phase is leading compared to the output. As before the phase detector develops an error voltage which varies the voltage controlled oscillator output so that both the input and output frequencies are same. Thus in steady state there exists small phase error which is just sufficient to detune the voltage controlled oscillator to the require frequency. The greater the phase to frequency gain of the forward path the smaller the steady state phase error which results from the given input frequency deviation.

Jitter:

Let us suppose that the phase of the incoming signal is fluctuating whereas its average frequency remains constant. The integrating action of the voltage controlled oscillator smooths this jitter if the rate of jitter is rapid. Also the low pass filter attenuates the jitter before it is applied to the voltage controlled oscillator.

If the amplitude of the jitter is large the phase detector goes through a discontinuity and hence the circuit slips N cycles ahead or behind the input signal.

If the rate of jitter is very slow the circuit tracks it and passes on to the output. If the jitter is caused by addition of white Guassian noise to the coherent signal, the loop responds only to the noise components around the coherent signal. This property allows the loop to lock on to the coherent signal of known frequency eventhough it is surrounded by strong wideband noise.

Quieting:

When the voltage controlled oscillator itself is jittering because of the internal noise it is reduced by the feedback. This is known as the quieting of the internal noise of the voltage controlled oscillator.

Discontinuities:

Suppose the input frequency of the incoming signal is increased until the phase error is equal to $+N\pi$ where N is the dividing ratio. A little increase beyond this point makes the comparator to go through a discontinuity making the phase error to be $-N\pi$. This will start decreasing the oscillator frequency and the phase error rapidly returns to $+N\pi$ and then jump to $-N\pi$ again. After sometime the error will settle down to a periodic behaviour with discontinuities at regular intervals. The output frequency must be somewhat less than the input frequency because the average error must be somewhat less than $+N\pi$. The frequency of the phase error will be the beat frequency between the input and output divided by N.

Steady state phase error:

When it is required to synchronise the loop with a frequency which is not identical with the voltage controlled oscillator's frequency then there exists a steady state phase error. The comparator converts this phase error into voltage which is utilised to tune the voltage controlled oscillator to the required frequency, which is identical to the input frequency.

The gain a is the conversion gain from phase error to frequency. It is the change in output frequency (in radians per second) that resulted from the change in phase error of one radian.

The mistuning frequency w_m is the difference between the input and output frequencies. Then the steady state phase error is $\phi_e = w_m/a$. It is obvious that the higher the a the smaller the phase error for a given mistuning frequency w_m.

Lock frequency:

This is defined as the maximum frequency that can be locked in synchronism with the voltage controlled oscillator. It is determined by maximum range of the phase comparator. In the limit $w_m = w_L$ = Lock frequency = $N\pi a$.

Phase error margin:

The phase error margin is defined as the margin between the steady state phase error and the error which will cause a discontinuity. So $\phi_{er} = N\pi - \frac{w_m}{a}$, where ϕ_{er} = phase error margin; and w_m/a is the steady state phase error. Since the gain of the sawtooth comparator doesnot depend on the phase error, the small signal performance of this comparator is independent of the steady mistuning. If no discontinuities are allowed the phase error margin

limits the permissible peak jitter amplitude.

Behaviour of the loop in the linear region:

The phase-locked loop acts like a linear feedback system as long as the phase error doesnot exceed the bounds $\pm N\pi$. Let the gains of phase detector, low pass filter and the voltage controlled oscillator be a_1, a_2, a_3 and their transfer functions be 1, H(s), and 1/s respectively. Also assume $a = a_1 \times a_2 \times a_3$. Therefore forward gain

$$U = a_1 \; a_2 \; H(s) \; a_3/s = \frac{a\,H(s)}{s}, \qquad (4.1)$$

and feedback factor B=1. Then the response of the output phase ϕ_o to the change in the input phase ϕ_i is given by

$$Y = \frac{\phi_o}{\phi_i} = \frac{U}{1+UB} = \frac{a\,H(s)}{s+aH(s)}. \qquad (4.2)$$

The phase error $\phi_e = \phi_i - \phi_o = \frac{s}{s+\,aH(s)}\;\phi_i$. (4.3)

Here it should be remembered that we have to measure the phase of the submultiple signals in radians of the original signals.

For a lead lag type of filter the transfer function H(s) is given by

$$H(s) = \frac{1+s\,T_2}{1+s\,T_1} \qquad (4.4)$$

Thus the transfer ratio

$$Y = \frac{1+s\,\tau_2/a}{1+s(1+\tau_2)/a + s^2\,\tau_1/a^2} \qquad (4.5)$$

where $\tau_1 = aT_1$ and $\tau_2 = aT_2$, and the phase error

$$\phi_e = \frac{\frac{s}{a}\,(1+s\,\tau_1/a)}{1+s\left(\frac{1+\tau_2}{a}\right)+s^2\,\tau_1/a^2} \qquad (4.6)$$

The denominator of the polynomials (4.5) and (4.6) is a second order polynomial of the form,

$$1 + s\,\frac{2z}{w_n} + s^2\left(\frac{1}{w_n}\right)^2 \qquad (4.7)$$

where $w_n = \frac{a}{\sqrt{\tau_1}}$ and $z = \frac{1}{2}\cdot\frac{\tau_2+1}{\sqrt{\tau_1}}$

w_n is the loop bandwidth or natural frequency of the loop and z is called as the damping factor. These parameters are particularly important in transient response to a step input of phase or frequency.

Pull-in frequency:

It is one of the very important parameters of the phase locked loop system. We can define pull-in frequency as the range of frequencies that can pull the oscillator into synchronism. In general this is smaller than the lock-in frequency.

The experimental determination of the pull-in frequency is as follows: The input signal is mistuned beyond the lock-in frequency. Then mistuning is slowly reduced until circuit locks in. When the tuning exceeds the lock range there are frequent discontinuities in the phase error and it appears to flicker. As the mistuning is slowly decreased the flicker rate decreases. When the mistuning is brought down to pull-in frequency the flicker mode becomes unstable. With the mistuning held at pull-in frequency the flicker mode slowly disappears and the circuit is pulled into synchronism.

Goldstein found an exact answer to the pull-in frequency w_p;

$$\frac{w_p}{N\pi a} = \frac{1-D}{\tanh(\frac{1}{2} z w_n T_o)} + (D)\tanh(\frac{1}{2} z w_n T_o) \quad (4.8)$$

where T_o is the critical period, is given by the smallest positive solution of

$$\sqrt{\tau_1}\sqrt{z^2-1}\ \frac{\tanh(\frac{1}{2} z w_n T_o)}{\tanh(\frac{1}{2}\sqrt{z^2-1}\, w_n T_o)}$$

$$= \sqrt{\tau_1}\, z - \frac{\tau_1}{\tau_2}\left(1-\sqrt{1-\frac{\tau_2}{\tau_1}}\right) = C_1 \quad (4.9)$$

and D is given by

$$D = \frac{C\sqrt{\tau_1}\,(z-1)-\tau_1(z^2-1)}{C_1^2-\tau_1(z^2-1)} \qquad (4.10)$$

For the underdamped case ($z<1$) the hyperbolic tangent can be replaced by the trignometric tangent.

We can see from (4.8) that the pull-in frequency is directly proportional to the lock frequency, $N\pi a$. For small signal performance of the loop, the parameters τ_1, τ_2 and a are constant and hence the pull-in frequency can be increased by increasing the counter ratio N without affecting other performance factors like noise bandwidth etc.

But there are two limitations on the count. ratio. Firstly for our analysis to be valid the submultiple frequency must be much higher than the cutoff frequency of the loop which is of the order of w_n. The second one is purely economics. Higher count ratios needs more equipment. For $\tau_2 \gg 1$ and $\tau_2/\tau_1 < 0.5$ the pull-in frequency approaches

$$w_p = N a\pi \frac{2}{\sqrt{3}}\sqrt{\frac{\tau_2}{\tau_1}} \qquad (4.11)$$

Seize frequency:

If the input frequency mistuning is less than the pull-in frequency the circuit will certainly be locked

into synchronism, but it may flicker for considerably long time before it goes into lock.

But in some applications like symbol synchroniser etc. it is important that circuit must go instantaneously into lock with the signal that has just started. We define the seize frequency w_s as the maximum mistuning of a suddenly connected signal that cannot cause a discontinuity after a initial phase jump.

The maximum initial phase jump that can be tolerated without cousing discontinuity is $N\pi$. The seize frequency is the value of mistuning for which the initial derivative of the phase error is zero, so that no discontinuity results. The seize frequency w_s is given by the formula

$$\frac{w_s}{Na} = \frac{\tau_2}{\tau_1} \qquad (4.12)$$

Settling time:

It is the time required for the phase error to settle to its steady state value after a change in input conditions. If no discontinuityoccurs, the settling time t_s may be estimated to be time at which the damping terms $e^{-z\, w_n t_s}$ decays to 0.1. Substituting for z according to (4.7)

$$t_s = \frac{4.6}{\tau_2 + 1}\ T_1. \qquad (4.13)$$

If the discontinuity is crossed, an additional time will

)e required to allow for the flicker to die out. During the period of each flicker a small charge is added to the filter capacitor which brings the voltage controlled oscillator frequency closer to input frequency. Hence the circuit will be pulled into synchronism.

Noise Bandwidth:

The phase controlled loop also reduces noise. Since the noise at the output is restricted to be narrow band it is convinient to express the noise as the bandwidth of an ideal filter (i.e. rectangular filter) that can pass the same mean square noise. The noise bandwidth can be computed from the following formula,

$$B = \int_0^\infty |G(w)|^2 \, dw, \qquad (4.14)$$

where G(w) is the normalised transfer function between the noise input and noise output and B is in radians per second.

In our particular case (i.e. when the oscillator is used to remove jitter) the transfer function G(w) is given by Y as given by (4.5). Let us call the jitter bandwidth as B_j.

Substitute (4.5) into (4.14) we get

$$\frac{B_j}{\pi a} = \frac{1}{2} \, \frac{1+\frac{\gamma_2^2}{\gamma_1}}{1+\gamma_2} \qquad (4.15)$$

We know $N\pi a$ is the lock frequency. An increase in N increases the lock frequency without changing B_j.

The normalized jitter bandwidth is $\frac{1}{2}$ for an R-C filter or for no filter. It can be seen that if τ_2^2/τ_1 much greater than 1 then the normalized jitter bandwidth approaches $\frac{1}{2}(\tau_2/\tau_1)$.

In this chapter we analysed many of the properties of the phase locked loop with a sawtooth comparator. Some of the properties like lock frequency, pull-in frequency and noise bandwidth are important in almost all the applications. Other properties like seized time and settling time etc. are important in certain other applications like ours i.e. in symbol synchronisation etc.

The following approximations are of much use in designing the phase locked loop with a sawtooth comparator.

Pull-in frequency:

$$w_p = N\pi a \times \frac{2}{\sqrt{3}} \sqrt{\tau_2/\tau_1} \text{ when } (\tau_2 \gg 1)$$

noise bandwidth

$$B_j = \frac{\pi a}{2} \tau_2/\tau_1$$

Lock-in-frequency

$$w_L = \pi N a.$$

CHAPTER 5

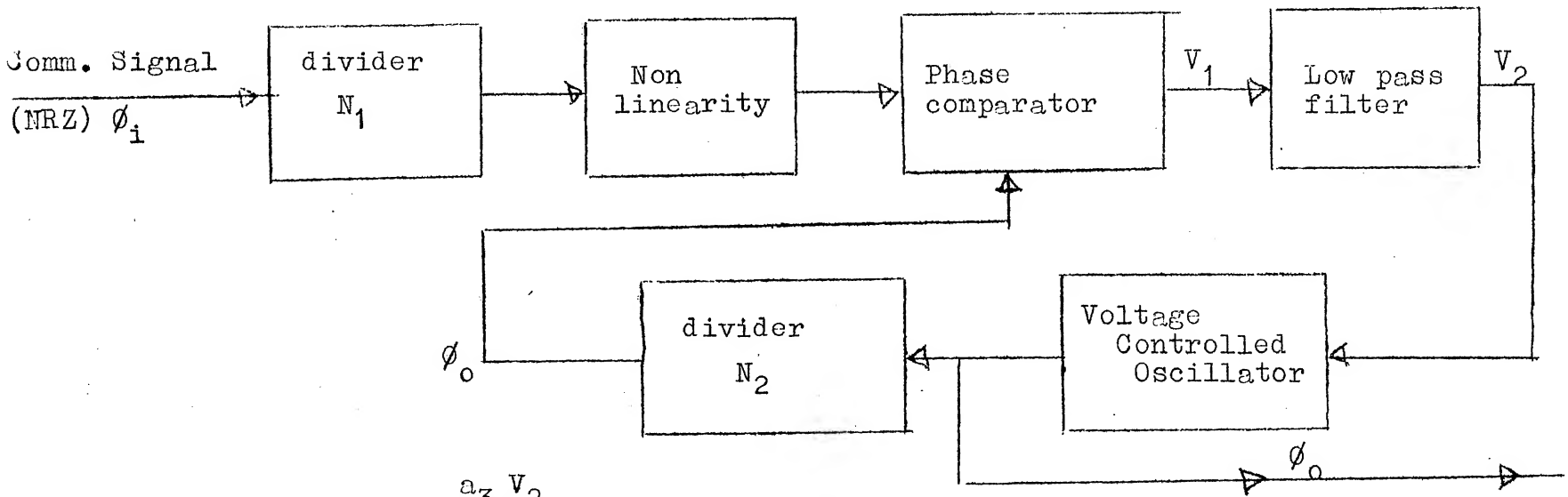
PHASE LOCKED LOOP SYMBOL SYNCHRONISER FOR DATA COMMUNICATION SYSTEMS

The incoming data stream contains the components of the clock signal which is used to generate the data stream at the transmitting end. Hence by using the phase locked loop we can extract the symbol synchronisation signal by making it lock in synchronism with the symbol synchronisation signal contained in the data stream. A basic block diagram of the phase locked loop symbol synchroniser is shown in the Fig. 5.1.

The various elements of the symbol synchroniser are, two dividers, a non-linearity phase comparator, low pass filter, voltage controlled oscillator. The significance of the frequency dividers in a phase locked loop already been discussed in the previous chapter.

Non-linear Element:

It is common practice to use non-return to zero (NRZ) signals in digital communications. A non-return to zero signal is one in which the signal stays at the continuous level for the full digit period and does not returns to zero through half way of the digit period. In the



$$\phi_e = \phi_i - \phi_o, \quad \phi_o = \frac{a_3 V_2}{s}, \quad U = \phi_o/\phi_e =$$

$$V_1 = f(\phi_e); \quad V_2 = a_2 H(s) V_1, \quad = \frac{a_1 a_2 a_3 H(s)}{s}$$

Fig. 5.1 Phase locked loop symbol synchronizer.

spectrum of NRZ signal there is a null at the digit rate. In order to generate components at the digit rate it is required to introduce a non-linearity in the signal path.

We can introduce the required non-linearity by various means. It can be a full wave rectifier, a full wave rectifer slicer, a monostable multivibrator, a square law rectifier, or any other device which is capable of doing any one of the above jobs. With a sawtooth type of comparator using monostable multivibrator for non-linearity may be an ideal one.

Phase Comparator:

The phase comparator is the error detector of the loop. It produces an output depending on the phase difference of the input and output signals of the loop. Basically there are five types of phase comparators which can be used in phase locked loops. They are sawtooth, linear gate, digital gate, early gate/late gate and counter digital/analogue comparators.

All the above mentioned comparators are more or less equal in performance. But the sawtooth comparator offers number of advantages compared to the other types of comparators. The advantages can be listed as below:

) It's output is linear for large values of phase error. In fact it's output remains linear for a phase difference of nearly one digit period.

2) Since it works on zero crossings it's gain doesn't depend on amplitude of input signals.

3) Since it's gain does not depend on the signal amplitude the small signal performance is independent of steady mistuning.

4) It has a large pull-in frequency at least twice that of a sinusoidal comparator of the same small signal performance.

Loop filter:

The loop filter is a law pass filter . With symbol synchroniser loops of various orders may be used. A first order loop results if there is no filter included i.e. the filter transfer function is unity. By using a lead-lag filter the loop becomes a second order loop. In this case we can choose damping factor and natural frequency of oscillation independently while making the loop gain as large as necessary in order to obtain good tracking performance. In addition we have to incorporate memory to the loop because the signal may fade or fail for short intervals. For this purpose we are using an active filter. The active filter is shown in Fig. 5.2.

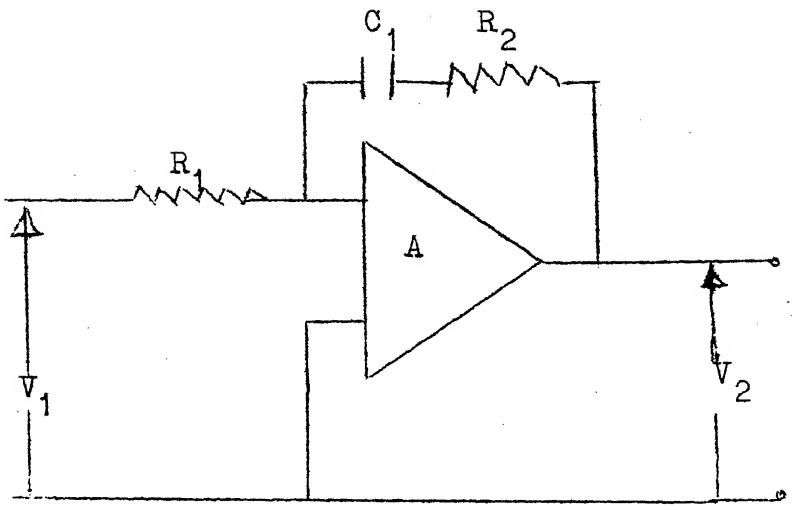
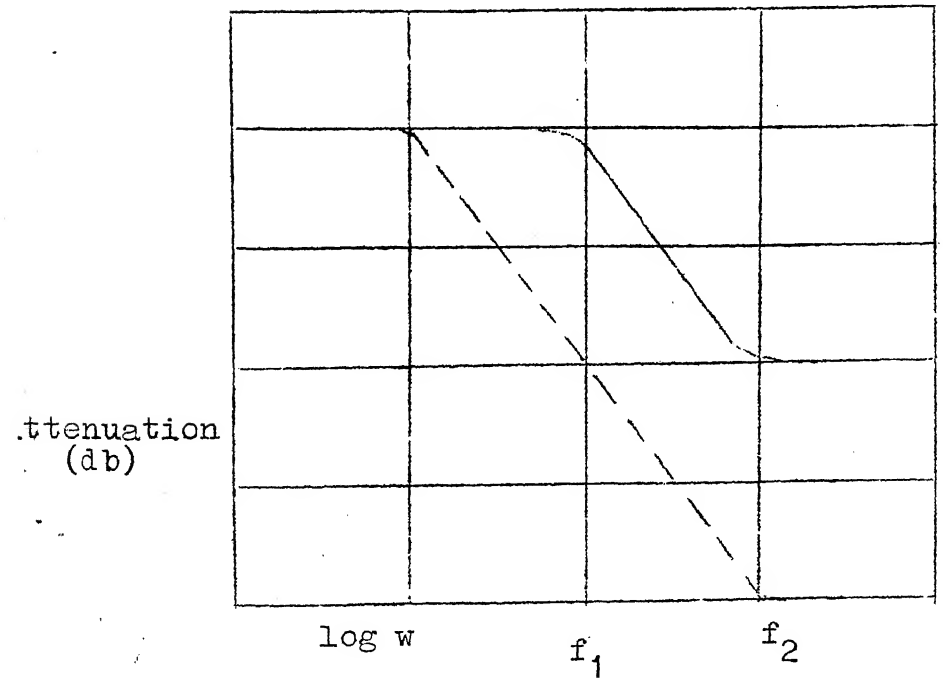


Fig. 5.2 a) lead-lag filter



$f_1 = 1/T_1 = 1/2 \quad (R_1+R_2)C_1$; $f_2 = 1/T_2 = 1/2 \quad R_2C_2$

High frequency gain $= \gamma_2/\gamma_1+\gamma_2$ (for passive filter)

$= \gamma_2/\gamma_1$ (for active filter)

Fig. 5.2 b) lead-lag filter response.

From the above discussion we understood that the synchroniser with a sawtooth comparator and active lead lag filter offers many desirable characteristics. So we selected the above elements for construction of the symbol synchroniser. The performance characteristics and design criteria of this type of symbol synchroniser are listed below.

Acquisition:

When the digit rate clock signal and the voltage controller oscillator are not in phase-lock, then synchronism can be achieved in two different circumstances.

1) If the loop bandwidth is greater than the difference between the input and output submultiple frequencies then the loop goes into lock almost instantaneously without slipping any cycles ahead or behind.

2) But if the loop bandwidth is smaller than the difference between the input and output submultiple frequencies, which is usually the case because of the requirements on noise and jitter performance of the loop, the acquistion time is unduly long; of the order of minutes even. But as far as our requirements are concerned both fast acquisition as well as good noise and jitter performance are equally important. In order to satisfy both the requirements two methods are

available in the literature namely, oscillator sweeping and bandwidth expansion.

Oscillator sweeping:

One method is to apply ramp to the voltage controlled oscillator's control terminal. When the voltage controlled oscillator frequency is within the fast acquisition range it automatically goes into lock. Once the lock is established the ramp voltage present will be made ineffective by the servo action of the loop. But if the loop goes out of lock the ramp voltage present will cause difficulties in reacquisition. Hence it is always desirable to switch off the ramp voltage once the lock is established.

Instead of the ramp a step voltage can be applied to the filter input. The step voltage will be converted into a ramp because of the integrating action of the loop filter. Thus applying step at the input of the filter is equivalent to applying ramp to the voltage controlled oscillator's control terminal. However when we use the step a little transient jump in the voltage controlled oscillator frequency is observed which is objectionable in certain applications. And so, we prefer the following.

Bandwidth expansion:

In this method two bandwidths for the loop are provided, a narrow bandwidth for good noise performance and a large bandwidth for the fast acquisition. If the bandwidth of the loop is made larger than the lock frequency and the difference between the submultiple frequencies lies within this range then the loop goes into lock very fast. When once the loop goes into lock the loop filter is switched to the other mode i.e. to the narrow band mode by switching the components of the loop filter. The voltage necessary to switch the filter to the narrow band mode from wide band mode can be derived from the lock indicator circuitry. A method of implementing the above principle is shown in Fig. 5.3, which is also the block diagram of the symbol synchroniser designed and fabricated. The test results also confirm to the advantages mentioned earlier in the report.

Tracking:

Once the loop is pulled into lock it tracks the input signal provided the jitter is small enough not to cause discontinuities. Good tracking performance is obtained if the phase error is kept small at all times. This can be improved by using the active filter because it increases the

1) To minimise the phase jitter in the output caused by the jitter in the input, the loop bandwidth must be as small as possible.

2) To minimise the phase jitter in the output caused by the jitter in the oscillator output caused by the internal noise of the oscillator, and to obtain large pull-in range a wide bandwidth loop is required.

The above two requirements are contradicting each other. So in designing the loop a compromise has to be found out depending on the requirements of a particular application.

Implementation:

We have already discussed the need for bandwidth expansion. So a dual filter symbol synchroniser has been constructed for obtaining fast acquisition as well as for good noise and jitter performance. The block diagram of the dual filter symbol synchroniser is shown in Fig. 5.3.

The incoming signal is shaped by the Schmitt Trigger. After frequency division of two by the input divider the signal is fed to the monostable multivibrator. The monostable multivibrator generates short pulses at every negative going edge of the incoming signal. Similarly the voltage controlled

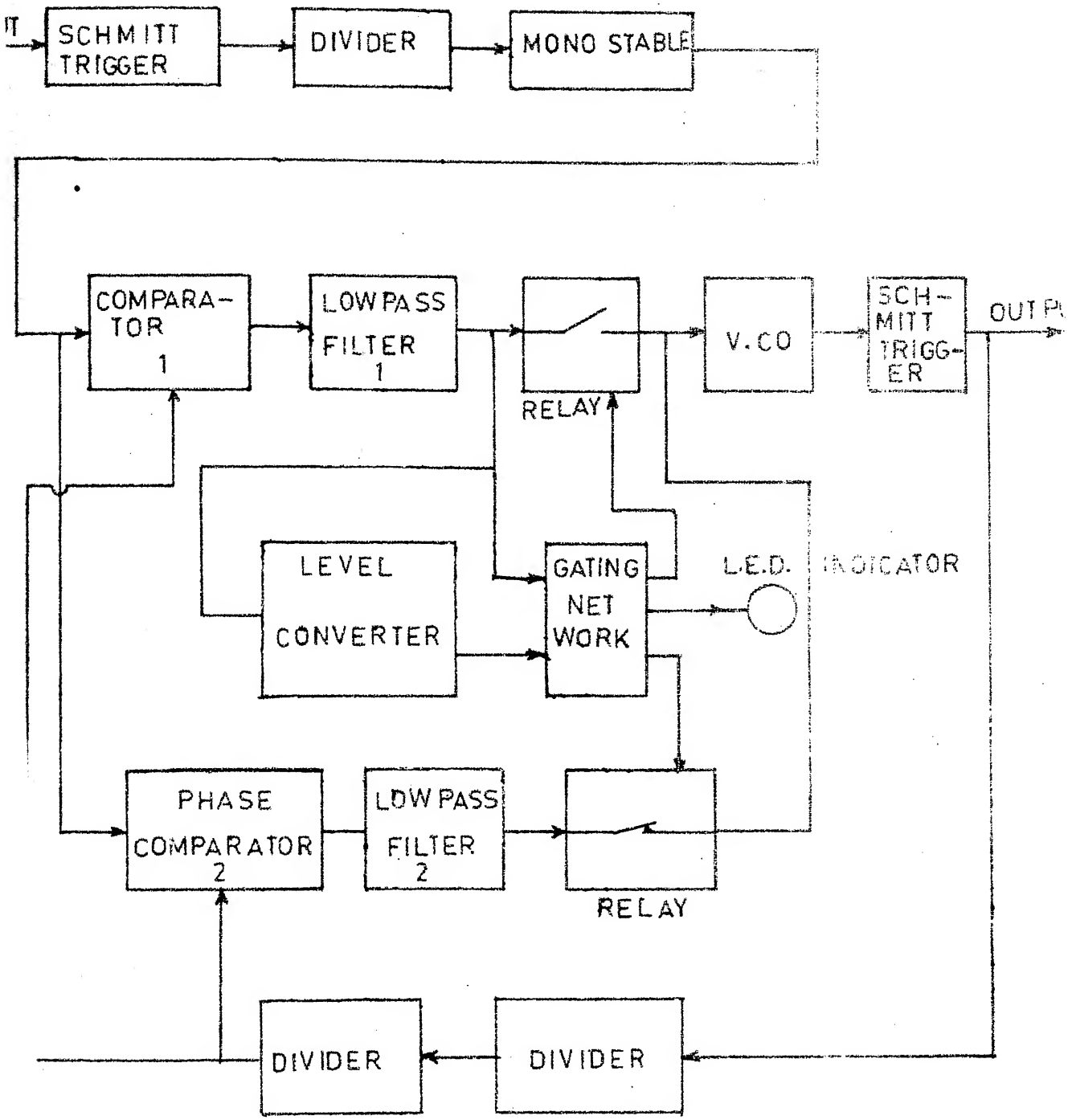


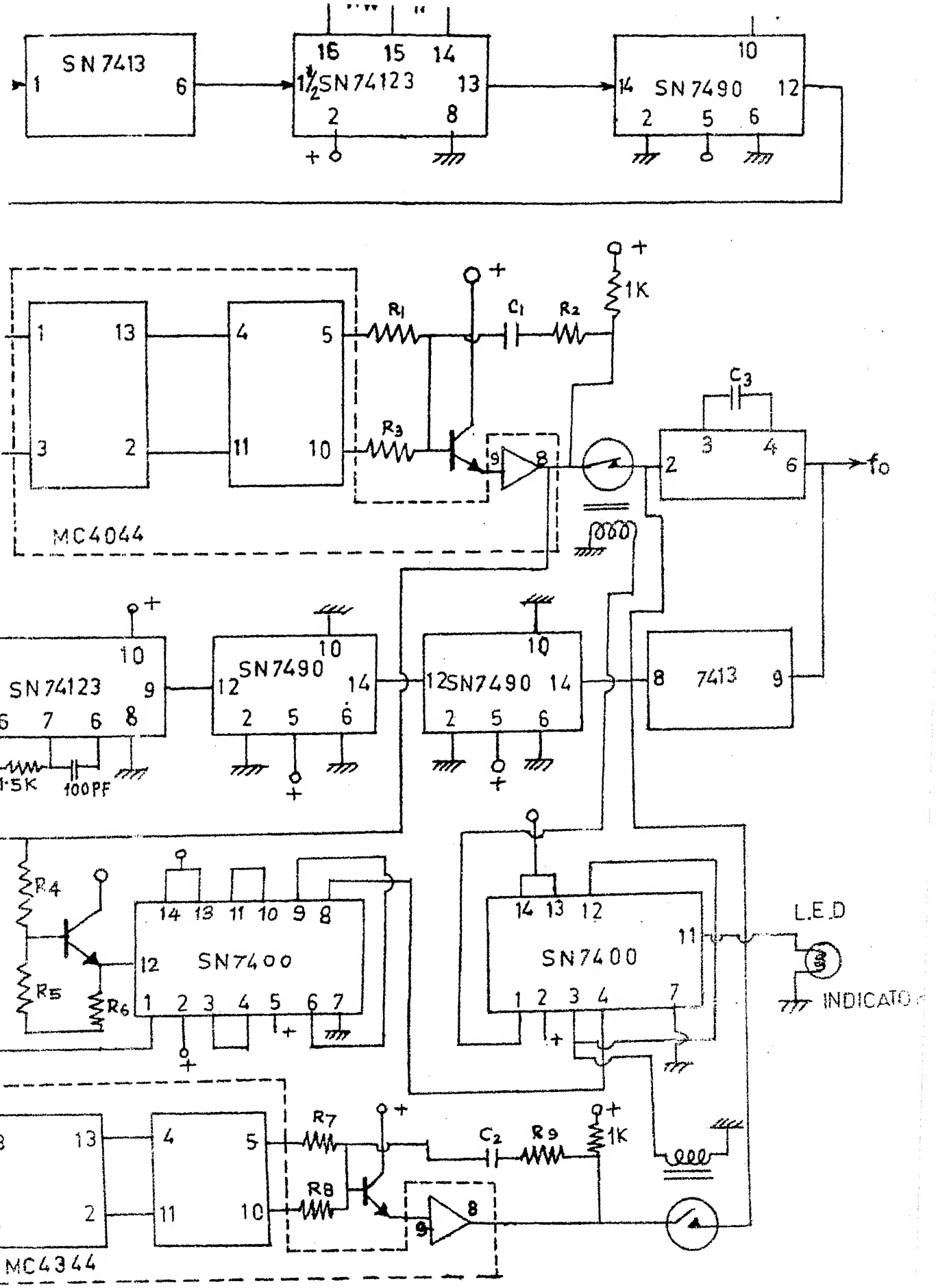
FIG.5.3 BLOCK DIAGRAM OF DUAL FILTER SYMBOL SYNCHRONIZER

oscillator's frequency after frequency division by 4 is fed to a monostable multivibrator. The output of this monostable multivibrator is given to the second input terminal of the phase comparator.

We used MC 4344/4044 I.C. chips for the phase comparators in the circuit. We will study about the above components in detail later in this chapter.

The output of comparator 1 after low pass filtering is fed to the voltage controlled oscillator control terminal via buffer 1 and read relay 1. The relays 1 and 2 keeps either comparator 1 low pass filter 1 and buffer 1 in the phase locked loop or comparator 2 low pass filter 2 and buffer 2 in the loop depending on the buffer output of the lamp indicating circuitry.

The output of the low pass filter 1 is used to activate the lock indicator circuitry. The output of the low pass filter 1 after level conversion using a transistor amplifier and nand gates is fed to the lamp via the lamp driver. The same output of the lamp driver will be used to switch an analog switch or a relay which in turn switches the phase locked loop from narrow bandwidth mode to large bandwidth mode or vice versa. The circuit diagram



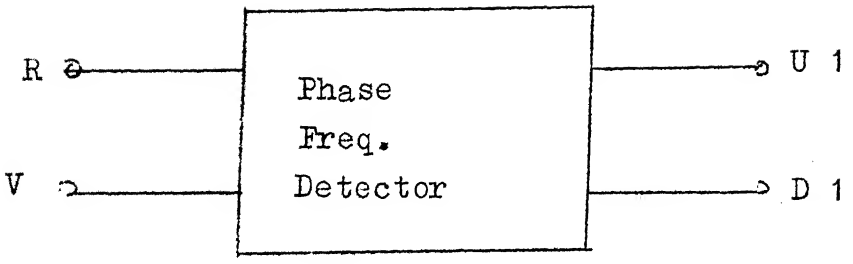
CKT DIAGRAM OF DUAL FILTER SYMBOL SYNCHRONIZE

is shown in Fig. 5.4.

Let us now study about the important components like phase comparator, voltage controlled oscillator etc. which we used in building the symbol synchroniser.

MC 4344/4044 Phase Comparator:

MC 4344/4044 integrated circuit chip is a phase detector. The flow table of the phase detector is shown in Fig. 5.5. It has got two inputs R and V and the output being U_1 and D_1. Lock up occurs where both the inputs U_1 and D_1 remain high. This occurs only when all the negative transitions on R, the reference input and V the variable or feed back input coincides. The circuit responds only to transitions and hence it's operation is independent of the input duty cycle or amplitude variations. Given in any particular condition the flow table in Fig. 5.5 can be used to determine the subsequent operations. The flow table indicates the status of U_1 and D_1 as the R and V inputs are varied. The numbers in the flow table which are in paranthesis are arbitrarily assigned that corresponds to stable states that can result for each input combination. The number without paranthesis refer to unstable condition. For a given input pair any one of the three stable states can



R-V 0-0	R-V 0-1	R-V 1-1	R-V 1-0	U1	D1
(1)	2	3	(4)	0	1
5	(2)	(3)	8	0	1
(5)	6	7	8	1	1
9	(6)	7	12	1	1
5	2	(7)	12	1	1
1	2	7	(8)	1	1
(9)	(10)	11	12	1	0
5	6	(11)	(12)	1	0

Fig. 5.5. Phase Detector Flow Table.

exist. For example, if R=1 and V=1 the circuit can be in one of the stable states (3), (7), or (11).

Use of the table in determining the circuit operation is illustrated in the Fig. 5.6. In the above timing diagram, the reference frequency is given to the R input and the input to V is the same frequency but lags in phase. Let us assume that stable state (4) as the initial condition. We can see from the timing diagram and flow table, where the circuit is in stable state (4),the outputs U_1 and D_1 are '0' and '1' respectively. The next input is R-V = '1'-'1'. Moving horizontally from stable state (4) under R-V = 1-0 to R-V = 1-1 column, state 3 is indicated. However this is unstable condition and the circuit will assume the state indicated by moving vertically in the R-V = 1-1 column to stable state (3). During this time outputs U_1 and D_1 remain unchanged. The next input to R-V is 0-1; moving horizontally to the R-V =0-1 column, stable state (2) is indicated. Still there is no change in outputs U_1 and D_1. The next input to R-V is 0-0 corresponding to the unstable state 5 is indicated. Moving vertically to stable state (5), the output now changes states to U_1-D_1=1-1. The next input change,R-V=1-0 drives the circuit to stable state (8), with no change in U_1 or D_1. The next input R-V =1-1 leads to the stable state (7) with

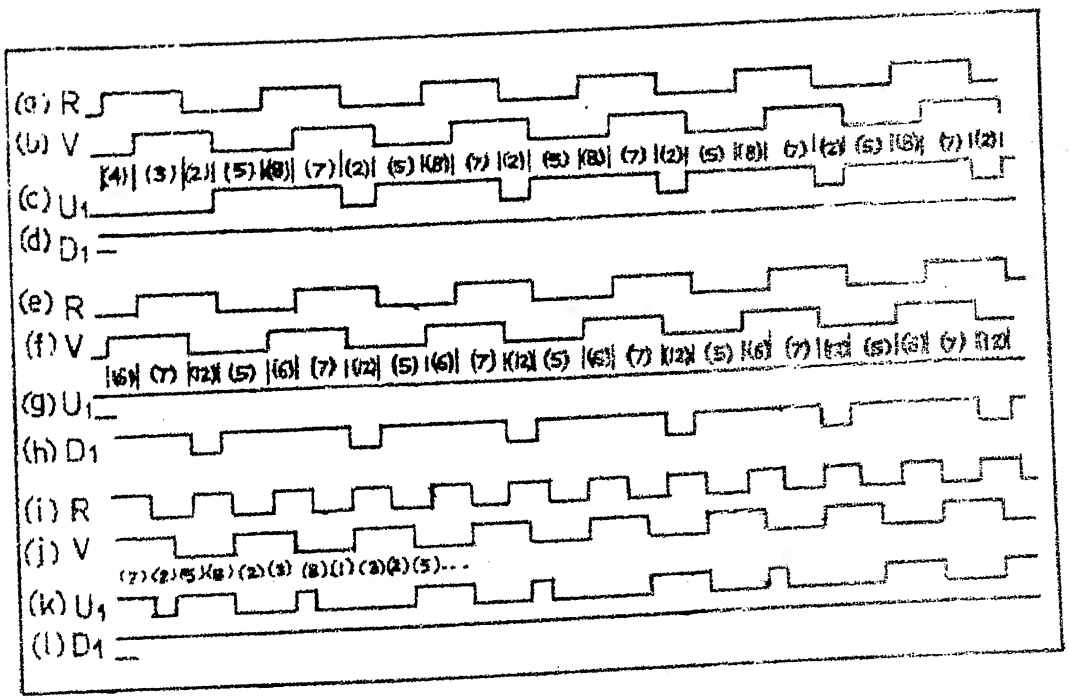


FIG.5.6 PHASE DETECTOR TIMING DIAGRAM

no change in the outputs. The next two inputs state changes cause U_1 to go low between the negative transitions of R and V. As the input continues to change, the circuitry moves repeatedly through stable states (2),(5),(8),(7),(2) etc. as shown and a periodic wave form is obtained on the U_1 terminal while D_1 remains high.

A similar result is obtained if V is leading with respect to R except that the periodic wave form now appears on D_1 as shown in the rows e-h of the timing diagram. In each case the average value of the resulting waveform is proportional to the phase difference between the two inputs. In closed loop applications the error signal for controlling the voltage controlled oscillator is obtained by translating and filtering these waveforms. In rows i-l of the timing diagram shows the results obtained when R-V are seperated by a fixed frequency difference. In this case, the U_1 output goes low when R goes low and stays in that state until negative transition on V occurs. The resulting waveform is similar to the fixed phase difference case, but now the duty cycle of the U_1 waveform varies at a rate proportional to the difference frequency of the two inputs, R and V. It is this characteristic that permits the MC 4344/4044 to be used as a frequency discriminator. If the signal on R has been frequency modulated

and if the loop bandwidth is selected to pass the deviation frequency but reject R and V, the resulting error voltage applied to the voltage controlled oscillator will be the recovered modulation signal.

Followed by the phase detector, MC 4344/4044 I.C. chip contains a charge pump and an operational amplifier. Let us study them one by one.

Charge Pump:

The circuit diagram of the charge pump is shown in Fig. 5.7. The operation is as follows. There will be a pulse wave-form on either P_d or P_u depending on the phase frequency relationship of R and V. The charge pump serves to invert one of the input waveforms (D_1) and translates the voltage levels before they are applied to the loop filter. When P_d is low and P_u is high, Q_1 will be conducting in the normal direction and Q_2 transistor will off. Current will be flowing through transistor Q_3 and diode CR_2; the base of transistor Q_3 will be two V_{be} (base to emitter voltage) drops above ground or approximately 1.5 volts. Since both of the resistors connected to the base of the transistor Q_3 are equal, the emmiter of transistor Q_4 will be approximately 3.0 volts. For this condition the emitter of transistor Q_5 will be one V_{be} below this voltage or about 2.25 volts.

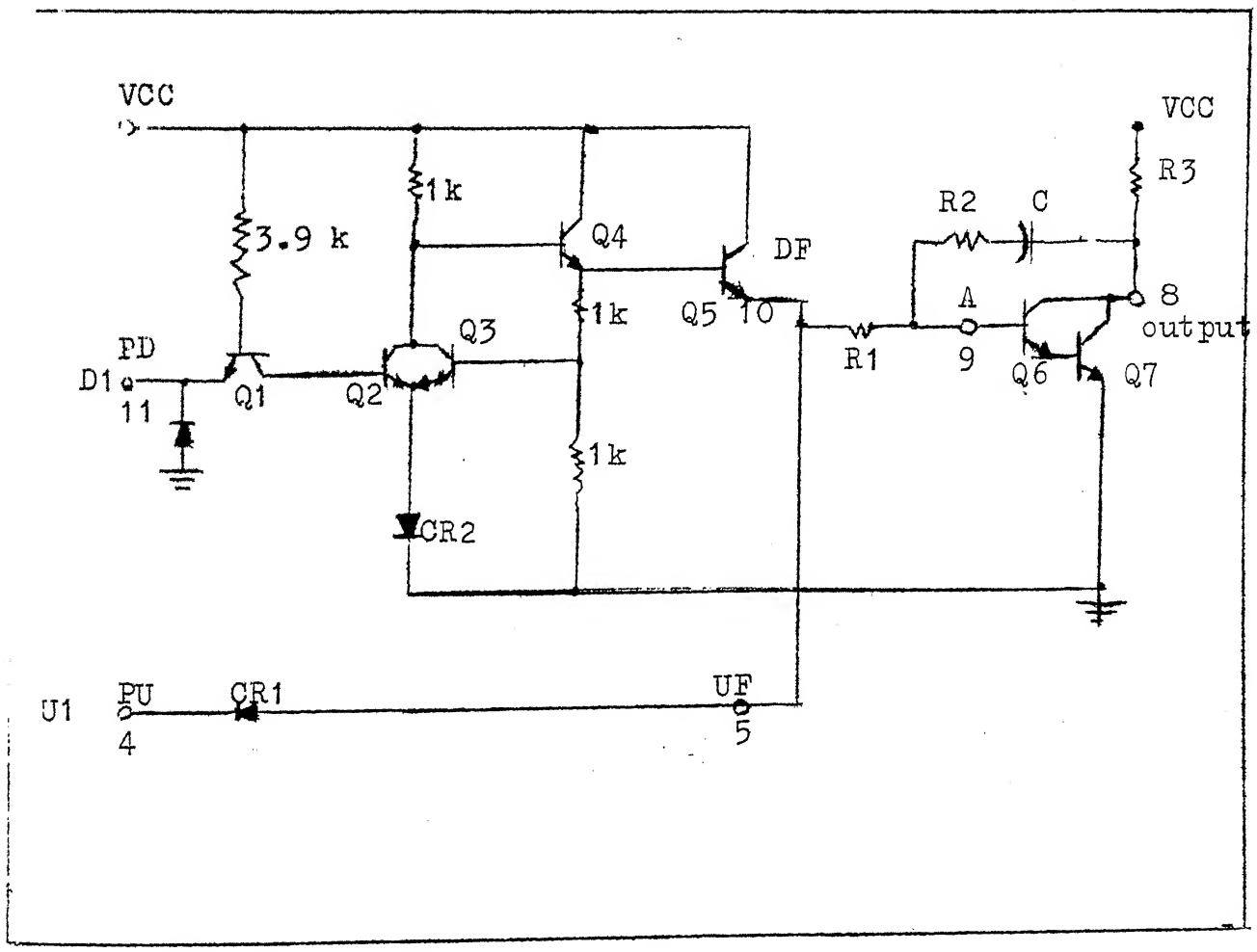


Fig. 5.7. Circuit Diagram of Charge Pump alongwith Filter.

Since the P_u input to the charge pump is high (>2.4 volts) and CR_1 diode will be reverse biased. Therefore transistor Q_5 will be supplying current to transistor Q_6. This will tend to lower the voltage at the collector of transistor Q_7, resulting in an error signal that lowers the voltage controlled oscillator frequency as required by a pump down signal.

When P_u is low and P_d is high, the diode CR_1 is forward biased and uF will be approximately one V_{be} above ground. With P_d high, transistor Q_1 conducts in the reverse direction supplying base current for transistor Q_2. When transistor Q_2 is conducting transistor Q_4 is prevented from supplying base drive to transistor Q_5. With transistor Q_5 cutoff and uF low there is no base current for transistor Q_6 and the voltage at the collector of transistor Q_7 moves up, resulting in an increase in the voltage controlled oscillator operating frequency as required by a pump up signal.

When both inputs to the charge pump are high (zero phase difference) both CR_1 diode and the base emitter junction of transistor Q_5 are reverse biased and hence no change in the output of the charge pump. The output of the charge pump varies between one V_{be} and three V_{be} as the phase difference of R and V varies from -2π to $+2\pi$. When we remove the high frequency components by filtering, the phase detector

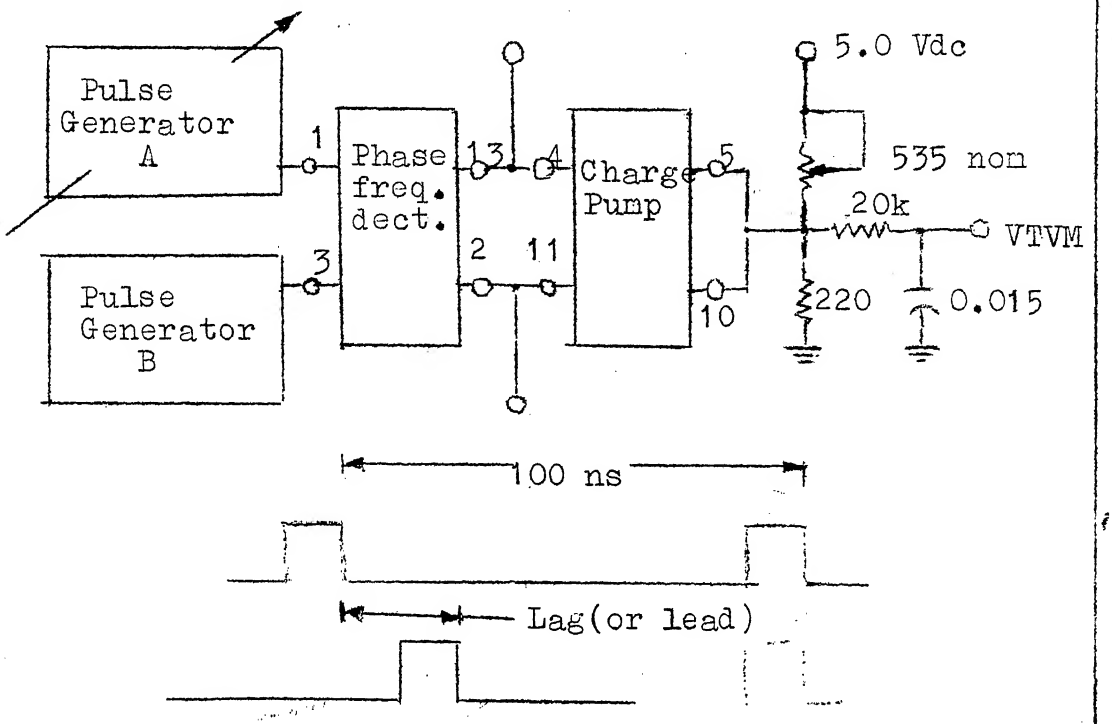
transfer function K_{ϕ} is approximately equal to 0.12 volts/ radian. The phase detector test circuit as well as its characteristic is shown in Fig. 5.8.

To get the specified gain constant of 0.12 volt/ radian we must use proper amplifier/filter combination. It can be observed from the phase detector characteristic that the pump delivers about 2.25 volts on the positive swings and 0.75 volts on negative swings for a no mean pump value of 1.5 volts. If the filter amplifier is biased to threshold at 1.5 volts, then the pump up and pump down voltages have equal effects.

Operational Amplifier:

MC 4344/4044 IC chip is provided with an operational amplifier, so that it can be utilised in the active filter needed for phase locked loop. It can be effectively used in the active filter provided its limits are observed.

The circuit configuration is illustrated in the Fig. 5.9 alongwith the filter components. The limitations on the use of the operational amplifier is due to the finite gain of the stage and other non-ideal characteristics. Typical voltage gain of the stage is about 30. The finite gain for the amplifier is provided intentionally because



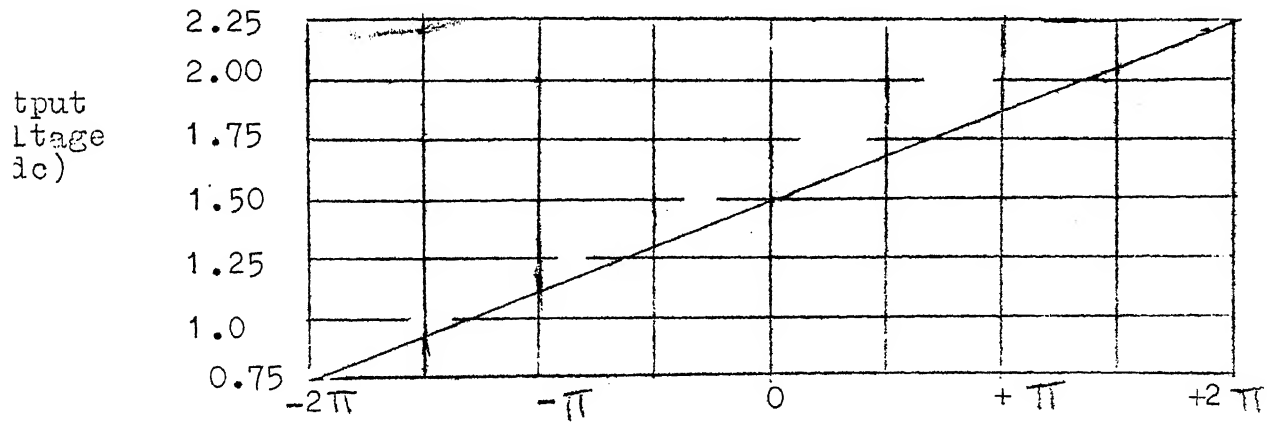


Fig. 5.8. Phase Detector Test Circuit and its Characteristic.

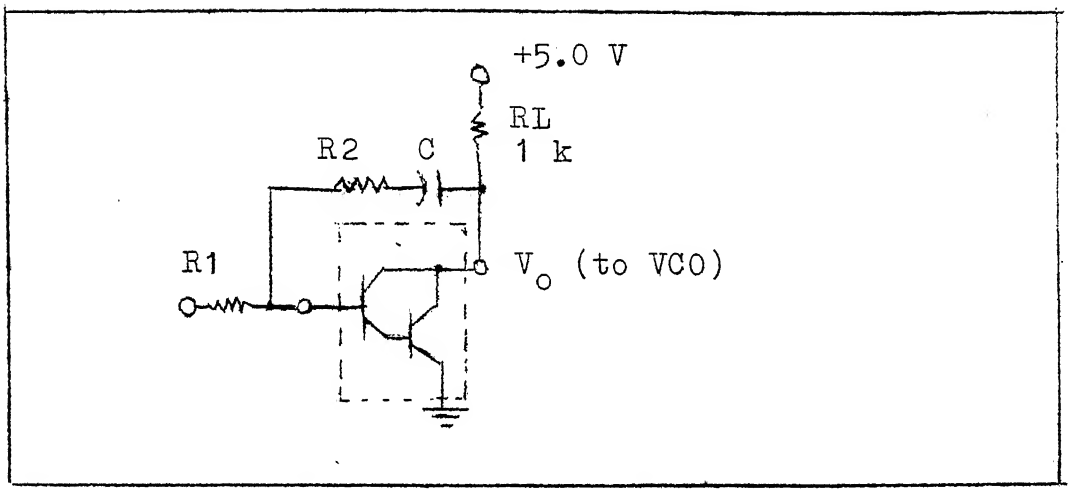


Fig. 5.9. MC 4344/4044 Loop Amplifier in Filter Configuration.

1) The amplifier/filter gain is an indication of how much the phase error exists between the input frequency f_{in} and output frequency f_{out} and filter characteristic shapes the capture range and transient performance. A low gain amplifier of simplicity is usually used since many designs are constrained by making f_{in} equal to f_{out} rather than the phase error.

2) Unnecessary high gain to the filter amplifier is often a source of trouble in linear loops especially when the loop is out of lock. If the amplifier output swing is not adequately restricted , then integrating operational amplifier latch up in time and effectively opens the loop.

Thus for proper operation the following limits has to be followed: (a) $R_2 > 50$, (b) $R_2/R_1 \leq 10$ (c) $1K < R_1 < 5K$.

MC 4324 Voltage Controlled Multivibrator:

The MC 4324 voltage controlled multivibrator can be variable over a range of 3.5 to 1 frequency range with an input d.c. control voltage of 1.0 to 5.0 voltage. It has got a maximum operating frequency of 25 MHz at 25°C. It consumes about 150 mw of power.

Standard Design Practices in using MC 4324:

1. Pins 5, 7, and 9 must be grounded.

2. Use capacitors with less than 50 nA leakage at plus and minus 3.0 volts. Capacitance values of 15 pF or greater are acceptable.

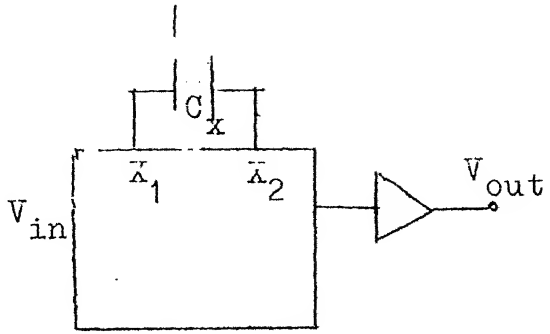
3. When operated in the free running mode, the minimum voltage applied to the d.c. control input should be 60% of VCC for good stability. The maximum voltage at this input should be VCC +0.5 volt.

4. When used in a phase locked loop, the filter output should have a minimum d.c. control input voltage of 1.0 volts and a maximum voltage of VCC +0.5 volt. The maximum instruction may be waived if the output impedance of the driving device is such that it will not source more than 10 mA at a voltage of VCC +0.5 volts.

5. The power supply for this device should be bypassed with a good quality RF type capacitor of 500 to 1000 pF. Bypass capacitor lead lengths should be kept as short as possible. For best results, power supply voltage should be maintained as close to +5 volts as possible. Under no circumstances should the design require operation with a power supply voltage outside the range of 5.0 volts $\pm$ 10%.

External Control Capacitor (C_x) Determination:

The operating frequency of this multivibrator can be controlled by a external capacitor connected between the terminals X_1 and X_2. This is shown in Table 5.1. A tuning ratio 3.5:1 can be obtained upto a maximum frequency of 25 MHz. An improvement in tuning ratio can be achieved by providing a variable tuning capacitor to facilitate initial alignment of the circuit.



$$\text{with } C_x = \frac{K_1}{f_{oH}} - 5$$

$$f_{oL} < \frac{K_2}{C_x}$$

TA	VCC	Values of K				
		1	K_2	K_3	K_4	K_5
25°C	5.0V	385	150	600	110	1.0
±3°C	5.0V ±5%	325	175	680	125	1.14
	5.0V ±10%	290	190	750	140	1.25

Table 5.1. External Control Capacitor value Determinations

CHAPTER 6

CONCLUSIONS

The objective of this report was to study and demonstrate the feasibility of acquisition of synchronization signals.

After studying different methods and techniques of synchronization the phase locked loop technique has been selected because of the requirement to construct a highly accurate symbol synchronizer that can be used universally at various frequencies.

Eventhough various types of comparators like, sawtooth, linear gate, digital gate early gate/late gate and counter digital/analog converter comparators, which are almost more or less similar in performance, are available, a sawtooth comparator is used for fabrication because of its inherently large linear range, which is responsible for its relatively superior performance.

To test the symbol synchronizer fabricated a binary data signal is applied to the input of the symbol synchronizer from the pseudo random binary signal generator. The output obtained from the symbol synchronizer is the synchronization

clock which is equal to the clock frequency, by which the data signals are generated. The data signal is in phase with the synchronization signal. The oscilloscope waveforms of the data signals, the clock signal which is used to generate the data signals and the synchronization signals obtained from the symbol synchronizer are shown in Fig. 6.1.

We can clearly visualise from Fig. 6.1 that the frequency of the data clock and synchronization clock are one and the same and all the waveforms are in phase.

Since the psuedo random binary sequence generator can generate sequences only with 1 MHz frequency signal, the symbol synchronizer was tested for frequencies only upto ≈1 MHz. By varying the capacitor of the voltage controlled oscillator the loop can be set to operate at the required frequency. We can infact use the above circuit easily upto 10 MHz.

Once the symbol synchronizer acquired the lock it followed all the changes in the input data signal. There is no meaning in measuring the accuracy of the loop because under lock conditions the output followed the input and had the same accuracy as the input.

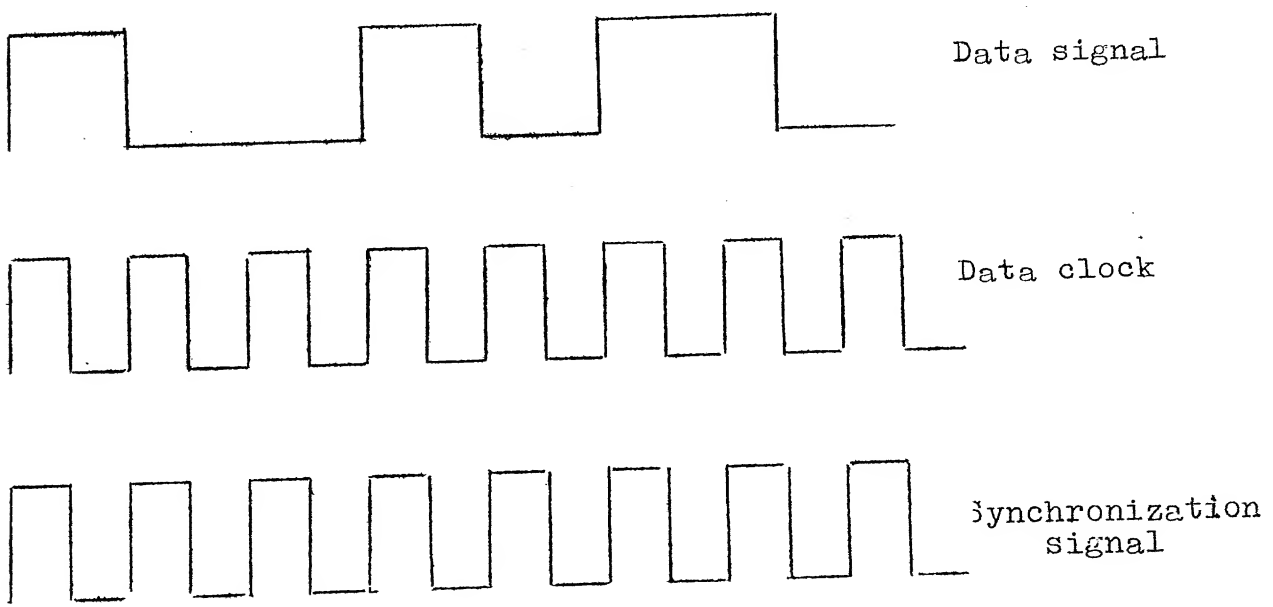


Fig. 6.1. Oscilloscope waveforms of data signals, data clock and synchronization clock signals.

With jitter free input to the symbol synchronizer the output jitter is almost nil.

Thus the choice of the selection of technique for fabricating the symbol synchronizer depends on a particular application. If a highly precision symbol synchronizer is required the choice is to go for phase locked loop symbol synchronizer.

While switching over the symbol synchronizer from acquisition mode (wide bandwidth mode) to the tracking mode (narrow bandwidth mode) it is advisable to introduce some delay otherwise it may so happen the switching may go on taking place between the two states especially at the transitions.

To denote the words and frames of data signals it is customary to transmit special signals in synchronous data transmission. These signals are extracted by the word and frame synchronization signal receivers and are used to reset the counters, to indicate the beginning or the end of the data word or data frame. The count of these

counters are increased or decreased by the symbol synchronization signal. As an extension of this a frame and word synchronization receivers may be constructed.

APPENDIX A

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APPENDIX B

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